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[3]	GCPU, DEBUG BUS
[4]	GCPU, VIDEO + PCIEX
[5]	GCPU, EEPROM + JTAG
[6]	GCPU, PLL PWR + FSB PWR
[7]	GCPU, PWR
[8]	GCPU, PWR
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[47]	VREGS, V5P0
[48]	VREGS, V3P3
[49]	VREGS, VEDRAM
[50]	VREGS, VMEM
[51]	VREGS, VCS
[52]	VREGS, LINEARS
[53]	VREGS, STANDBY SWITCHERS
[54]	BOARD, DECOUPLING
[55]	MARGIN, VMEM + VEDRAM
[56]	MARGIN, V3P3 + V5P0
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STINGRAY
REV 1.0
FAB C
RETAIL

Rules: (when possible)
* MSB-->LSB: top-->bottom
* When possible: inputs on left, outputs on right
* Page order: chip interfaces, termination, power, decoupling
* Avoid off-page connectors for on-page connections
* Bussed signals are grouped on symbols
* Unnamed nets are displayed with half-sized text
* Transmitter name used as prefix with RX and TX connections
* V_ prefix for voltage rail signal names
* _DP/_DN suffix for differential pairs
* _N suffix for active low or n junction
* _P suffix for p junction
* _EN suffix for enable
* CLK for clock, RST for reset
* PWRGD for power good
* Rev and fab set with custom variables. Tools->options->variables

[PAGE_TITLE=COVER PAGE]

DRAWING
Fri Jan 04 12:07:00 2013

PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	1/74	1/74	C	1.0

GCPU SETUP

25 IN CPU_RST_N

FT3T10 FTP 1

FT3T11 FTP 1

65 25 IN CPU_PWRGD

1 C5R11 360 PF 5% 50 V EMPTY 603 2

R4P5 2 1 1.27 KOHM 1% 402 EMPTY

1 R4P4 2 KOHM 1% 2 EMPTY 402

1 R3E10 10 KOHM 5% CH 402 2

1 C5R66 360 PF 5% 50 V EMPTY 603 2

CPU_RST_V1P1_N OUT 65

GCPU_VEJLE_BASE

U5E1 14 OF 17 IC

GCPU VERSION 1

D5 HARD_RESET_B

T5 POWER_GOOD

CHECKSTOP_B E5 CPU_CHECKSTOP_N OUT 65

22 IN CPU_CLK_DP R4D1 2 1 0 OHM 5% 402 CH

IN CPU_CLK_DP_R2 P2 CPU_CLK_DP

22 IN CPU_CLK_DN R4D2 2 1 0 OHM 5% 402 CH

IN CPU_CLK_DN_R2 P1 CPU_CLK_DN

VID6 C24 CPU_VREG_APS6 OUT 43

VID5 B24 CPU_VREG_APS5 OUT 43

VID4 A24 CPU_VREG_APS4 OUT 43

VID3 C23 CPU_VREG_APS3 OUT 43

VID2 B23 CPU_VREG_APS2 OUT 43

VID1 A23 CPU_VREG_APS1 OUT 43

1 FTP FT7P8

1 FTP FT7P7

1 FTP FT7P6

1 FTP FT7P5

1 FTP FT7P4

1 FTP FT7P3

V_CPUCORE

1 R4R22 100 OHM 5% 2 EMPTY 402

1 R4R23 100 OHM 5% 2 EMPTY 402

DB4R3 1

DB4R2 1

CPU_DBG_RST_EN	INTERNAL PULLDN
GPU_DBG_RST_EN	INTERNAL PULLDN

CPU_DBG_RST_EN P5 CPU_DBG_RST_EN<DN>

GPU_DBG_RST_EN R5 GPU_DBG_RST_EN<DN>

OUT EDRAM_PSRO_DOUT N6 PSRO_DOUT

OUT CPU_PSRO0_OUT G7 PSRO0_OUT

V_CPUPLL

WHEN V_CPUPLL=1.83V
SET VGATE=1.20V
ACTUAL=1.202V

N: IF V_CPUPLL CHANGES
VGATE RESISTORS SHOULD BE ADJUSTED

1 R5T8 562 OHM 1% 2 CH 402

<DN>PULSE_LIMIT_BYPASS J6 CPU_LIMIT_BYPASS OUT

CPU_VGATE V6 V_GATE <DN>PLL_BYPASS F8 CPU_PLL_BYPASS OUT

1 R5T9 1.07 KOHM 1% 2 CH 402

OUT RESISTOR0_DP L7 RESISTOR0_DP

OUT RESISTOR0_DN M7 RESISTOR0_DN

SRVID A3 CPU_SRVID OUT 51

EFU_POWERON C1 VREG_EFUSE_EN OUT 52

OUT CPU_EXT_CLK_EN F7 EXT_CLK_EN<DN>

CPU_TINIT J7 TI_39_TINIT

GND E7 TE

CORE_HF_BGR_PLL M6 CORE_HF_BGR_PLL OUT

1 R4R21 200 OHM 5% 2 CH 402

X818336-001 BGA_2

6 LAYER ONLY SIGNALS

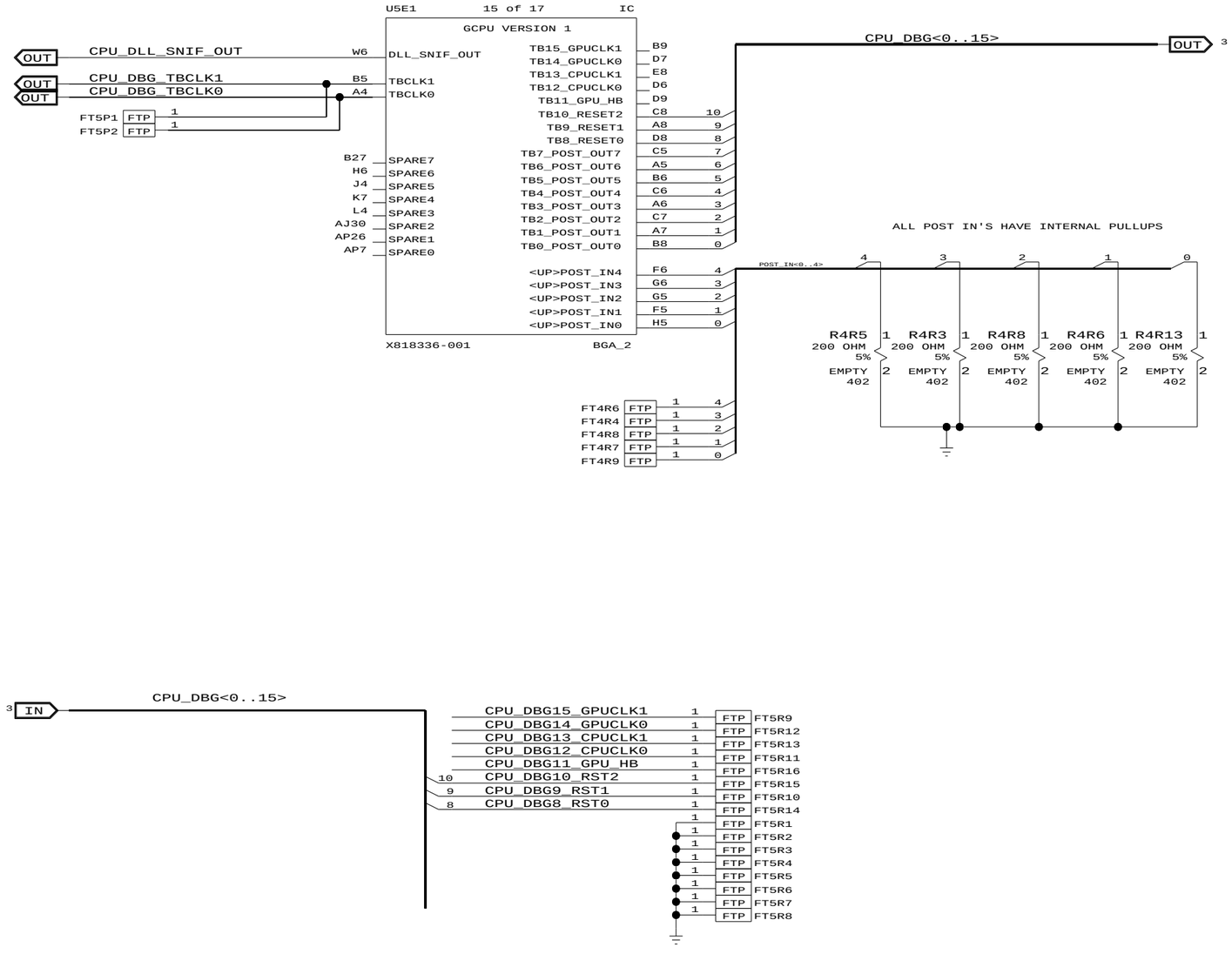
CORE_HF_BGR_PLL	6 LAYER ONLY; TP ONLY
CPU_LIMIT_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_PLL_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_CORE_HF_CLKOUT_DN	6 LAYER ONLY; TP ONLY
CPU_CORE_HF_CLKOUT_DP	6 LAYER ONLY; TP ONLY
CPU_EXT_CLK_EN	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_DLL_SNIF_OUT	6 LAYER ONLY; TP ONLY
CPU_VDDS0_DP	6 LAYER ONLY
CPU_VDDS0_DN	6 LAYER ONLY
CPU_VDDS1_DP	6 LAYER ONLY
CPU_VDDS1_DN	6 LAYER ONLY
RESISTOR0_DP	6 LAYER ONLY
RESISTOR0_DN	6 LAYER ONLY
EDRAM_PSRO_DOUT	6 LAYER ONLY

[PAGE_TITLE=GCPU SETUP]

DRAWING
Fri Jan 04 12:07:11 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 2/74	CSA PAGE 2/74	FAB C	REV 1.0

GCPU, DEBUG BUS

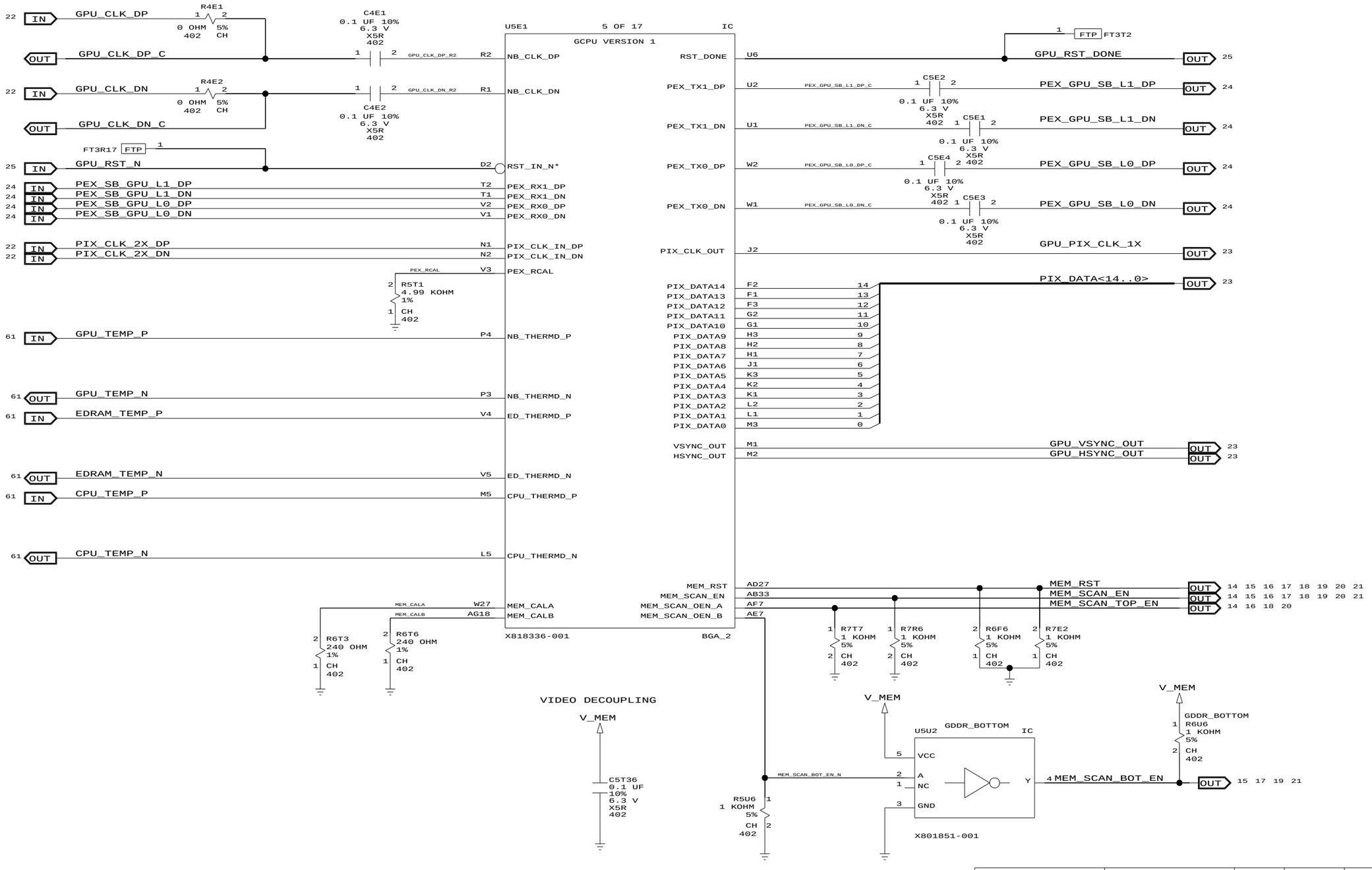


[PAGE_TITLE=GCPU, DEBUG BUS]

DRAWING
Fri Jan 04 12:07:11 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	3/74	3/74	C	1.0

GCPU, VIDEO + PCIEX

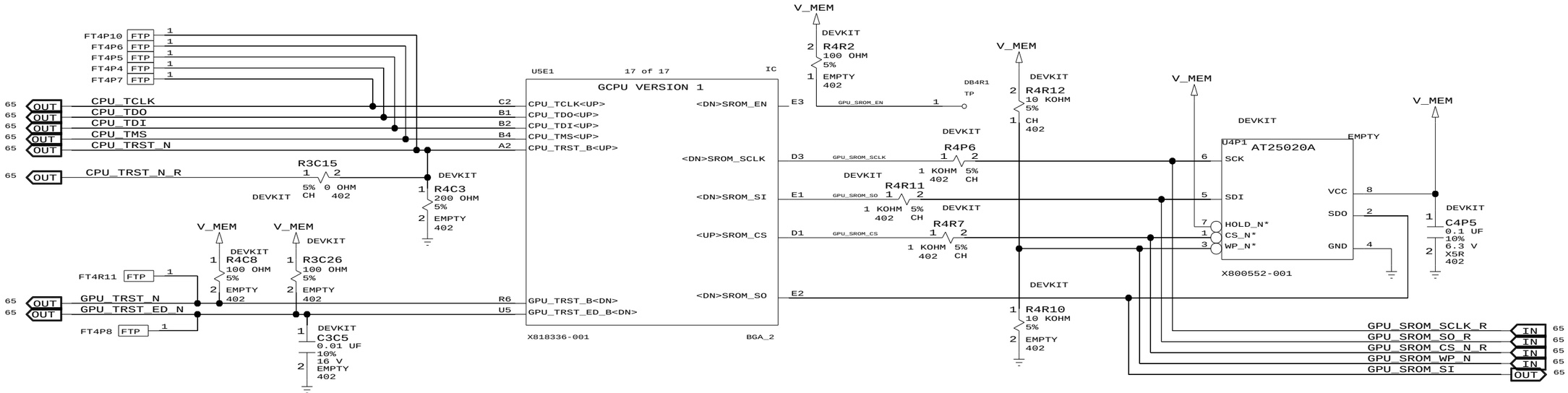


[PAGE_TITLE=GCPU, VIDEO + PCIEX]

DRAWING
Fri Jan 04 12:07:11 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	4/74	4/74	C	1.0

GCPU, EEPROM + JTAG



[PAGE_TITLE=GCPU, EEPROM + JTAG]

DRAWING
Fri Jan 04 12:07:12 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	5/74	5/74	C	1.0

GCPU, PLL POWER + FSB POWER

V_GPUPCIE V_CPUEDRAM V_CPUPLL

V_EFUSE U5E1 16 of 17 IC

GCPU VERSION 1

E4 VDDE

CORE_HF_CLKOUT_DP
CORE_HF_CLKOUT_DN

L6 CPU_CORE_HF_CLKOUT_DP
K6 CPU_CORE_HF_CLKOUT_DN

OUT CPU_VDDS1_DP
OUT CPU_VDDS1_DN
OUT CPU_VDDS0_DP
OUT CPU_VDDS0_DN

H25 VDDS1_DP
J26 VDDS1_DN
P7 VDDS0_DP
N7 VDDS0_DN

FB5R1 120 OHM 0.2A A 0.5DCR FB 603
C5R14 10 UF 20% 6.3 V X5R 805
ST5R1 SHORT
V_CPU_PVDDA_MEM D4 PVDDA_MEM
V_CPU_PVSSA_MEM C4 PVSSA_MEM

FB5T2 120 OHM 0.2A A 0.5DCR FB 603
C5T9 10 UF 20% 6.3 V X5R 805
ST5T1 SHORT
V_CPU_PVDDA_PEX U3 PVDDA_PEX
V_CPU_PVSSA_PEX U4 PVSSA_PEX

FB5R2 120 OHM 0.2A A 0.5DCR FB 603
C5R17 10 UF 20% 6.3 V X5R 805
ST5R2 SHORT
V_CPU_PVDDA_HS C3 PVDDA_HS
V_CPU_PVSSA_HS B3 PVSSA_HS

FB5T3 120 OHM 0.2A A 0.5DCR FB 603
C5T13 4.7 UF 10% 6.3 V X5R 603
ST5T2 SHORT
V_CPU_PVDDA_ED W5 PVDDA_ED
V_CPU_PVSSA_ED W4 PVSSA_ED

DB5R5
FB5R5 120 OHM 0.2A A 0.5DCR FB 603
C5R54 10 UF 20% 6.3 V X5R 805
ST5R5 SHORT
V_CPU_VDDA_RNG N4 VDDA_RNG
V_CPU_GNDA_RNG N3 GNDA_RNG

FB5R4 120 OHM 0.2A A 0.5DCR FB 603
C5R42 10 UF 20% 6.3 V X5R 805
ST5R4 SHORT
V_CPU_CORE_HF_VDDA_PLL J5 CORE_HF_VDDA_PLL
V_CPU_CORE_HF_GNDA_PLL K5 CORE_HF_GNDA_PLL

FB5R3 120 OHM 0.2A A 0.5DCR FB 603
C5R31 10 UF 20% 6.3 V X5R 805
ST5R3 SHORT
V_GPU_VDDA_PLL G4 GPU_VDDA_PLL
V_GPU_GNDA_PLL H4 GPU_GNDA_PLL

R3 VDD_VTT

FB5T1 120 OHM 0.2A A 0.5DCR FB 603
C5T4 4.7 UF 10% 6.3 V X5R 603
C5T6 0.1 UF 10% 6.3 V X5R 402
V_CPU_VDD_VTTA R4 VDD_VTTA

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OUT CPU_CORE_HF_CLKOUT_DP
OUT CPU_CORE_HF_CLKOUT_DN

DRAWING
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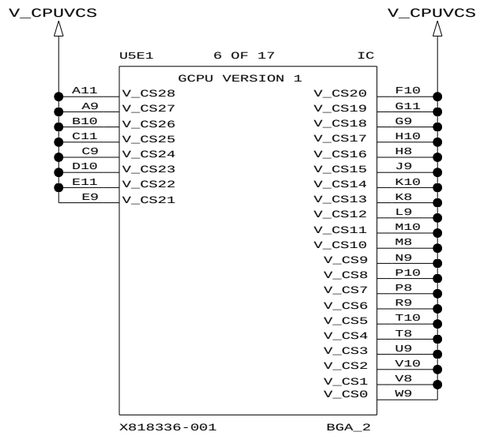
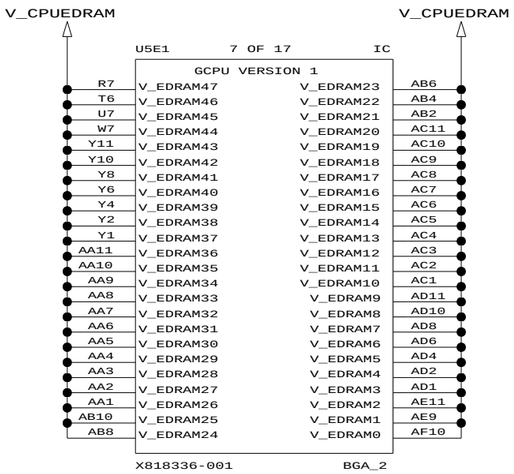
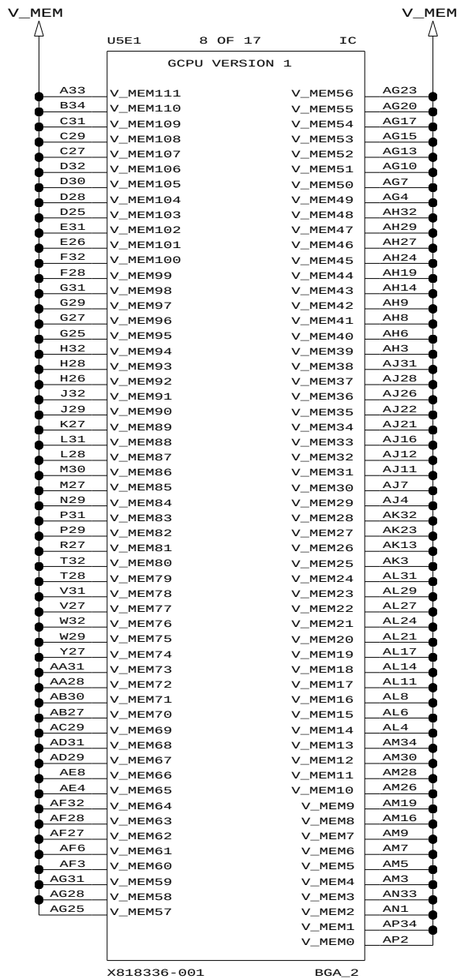
[PAGE_TITLE=GCPU, PLL POWER + FSB POWER]

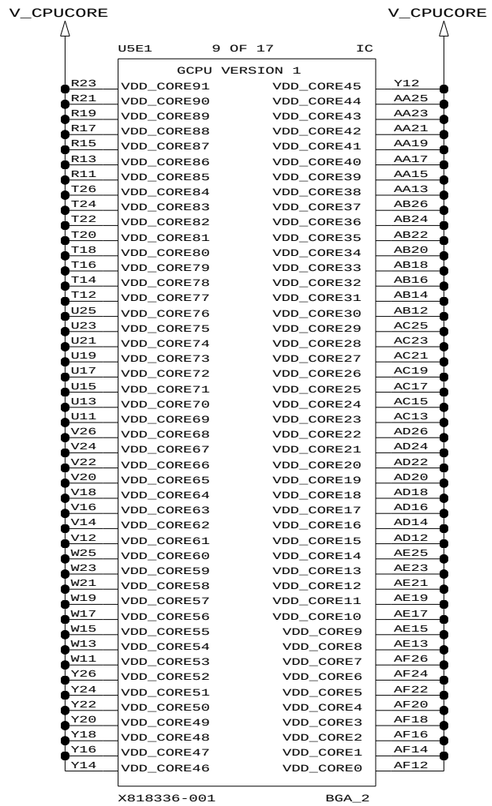
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 6/74	CSA PAGE 6/74	FAB C	REV 1.0

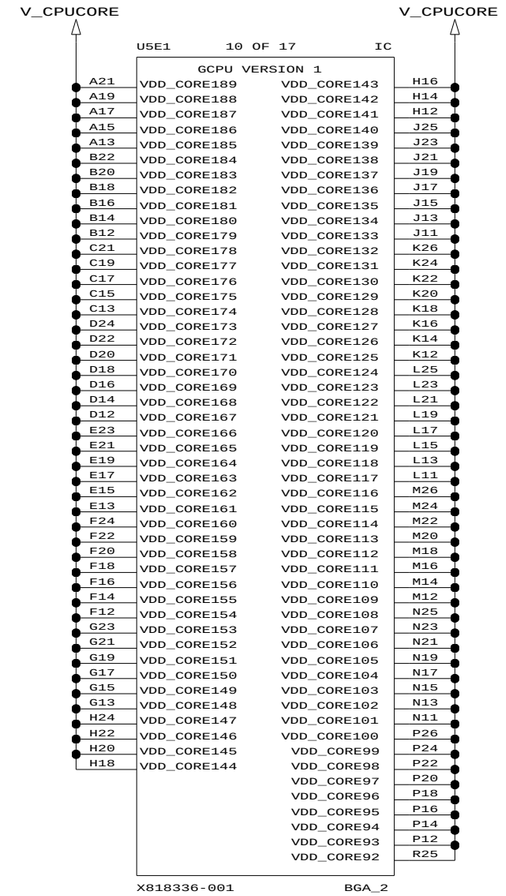
GCPU, POWER









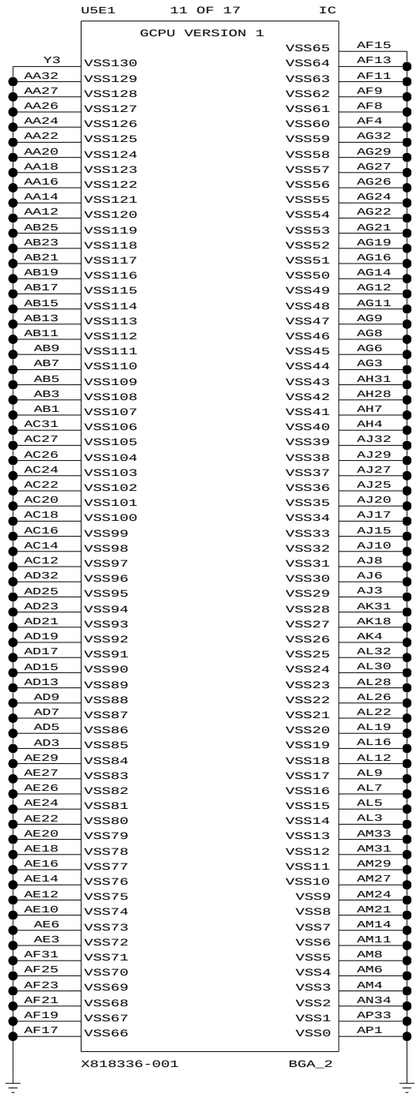


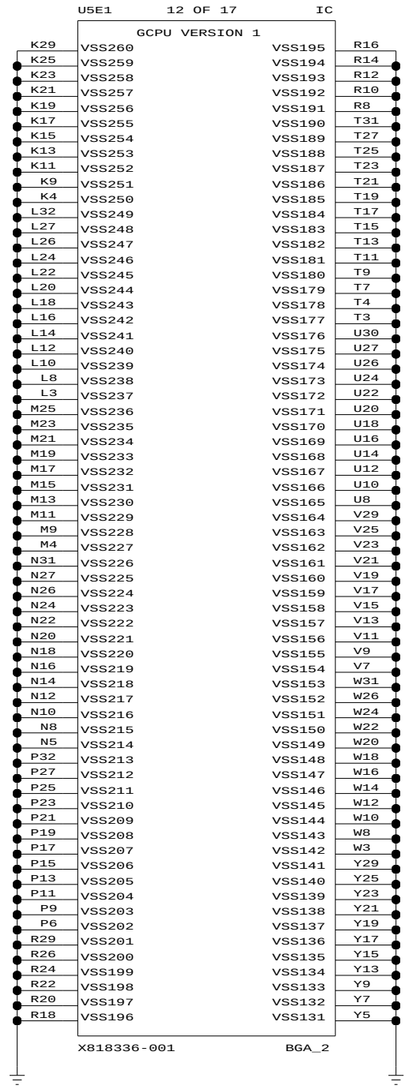
[PAGE_TITLE=GCPU, POWER]

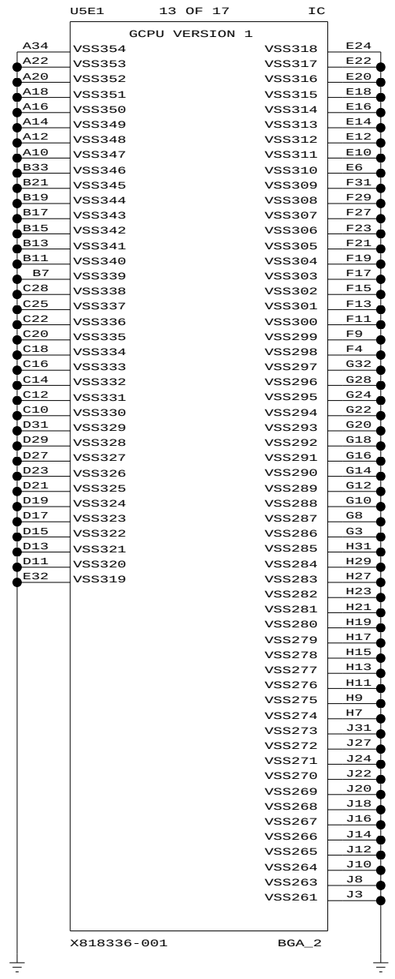
DRAWING
Fri Jan 04 12:07:12 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	7/74	7/74	C	1.0

GCPU, POWER







[PAGE_TITLE=GCPU, POWER]

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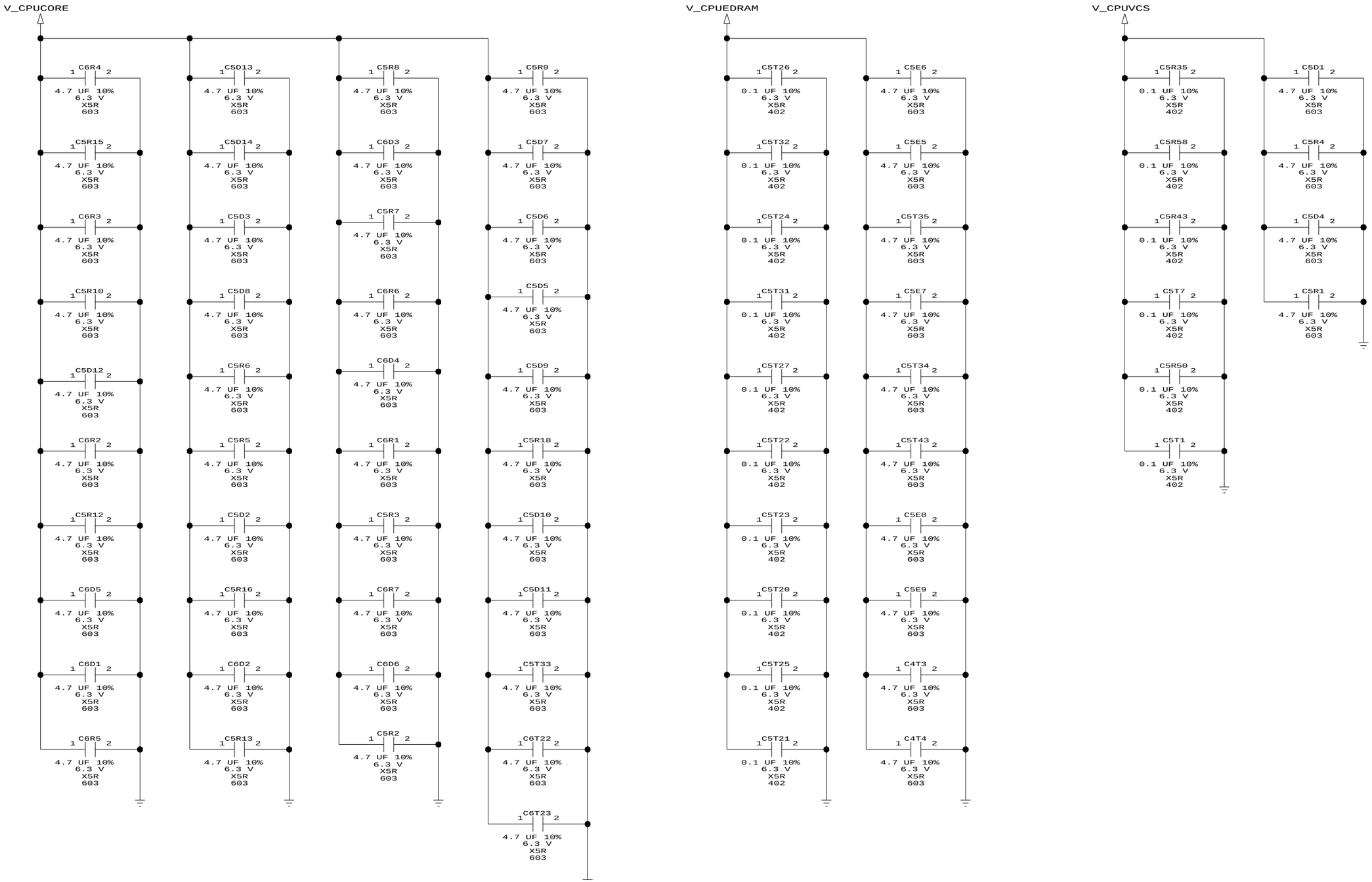
Fri Jan 04 12:07:12 2013

MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 8/74	CSA PAGE 8/74	FAB C	REV 1.0

GCPU, DECOUPLING

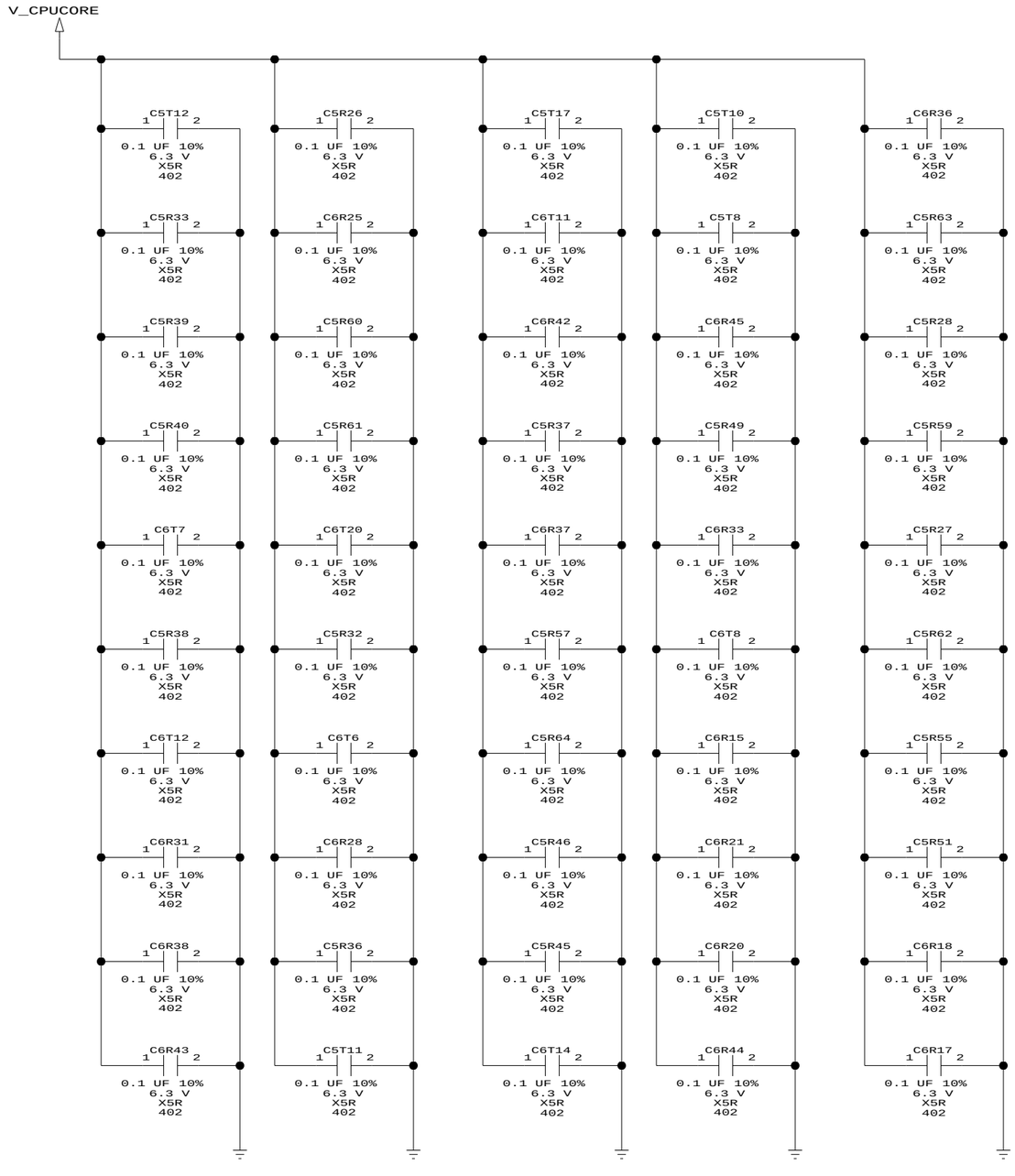


[PAGE_TITLE=GCPU, DECOUPLING]

DRAWING
Fri Jan 04 12:07:13 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	9/74	9/74	C	1.0

GCPU, DECOUPLING

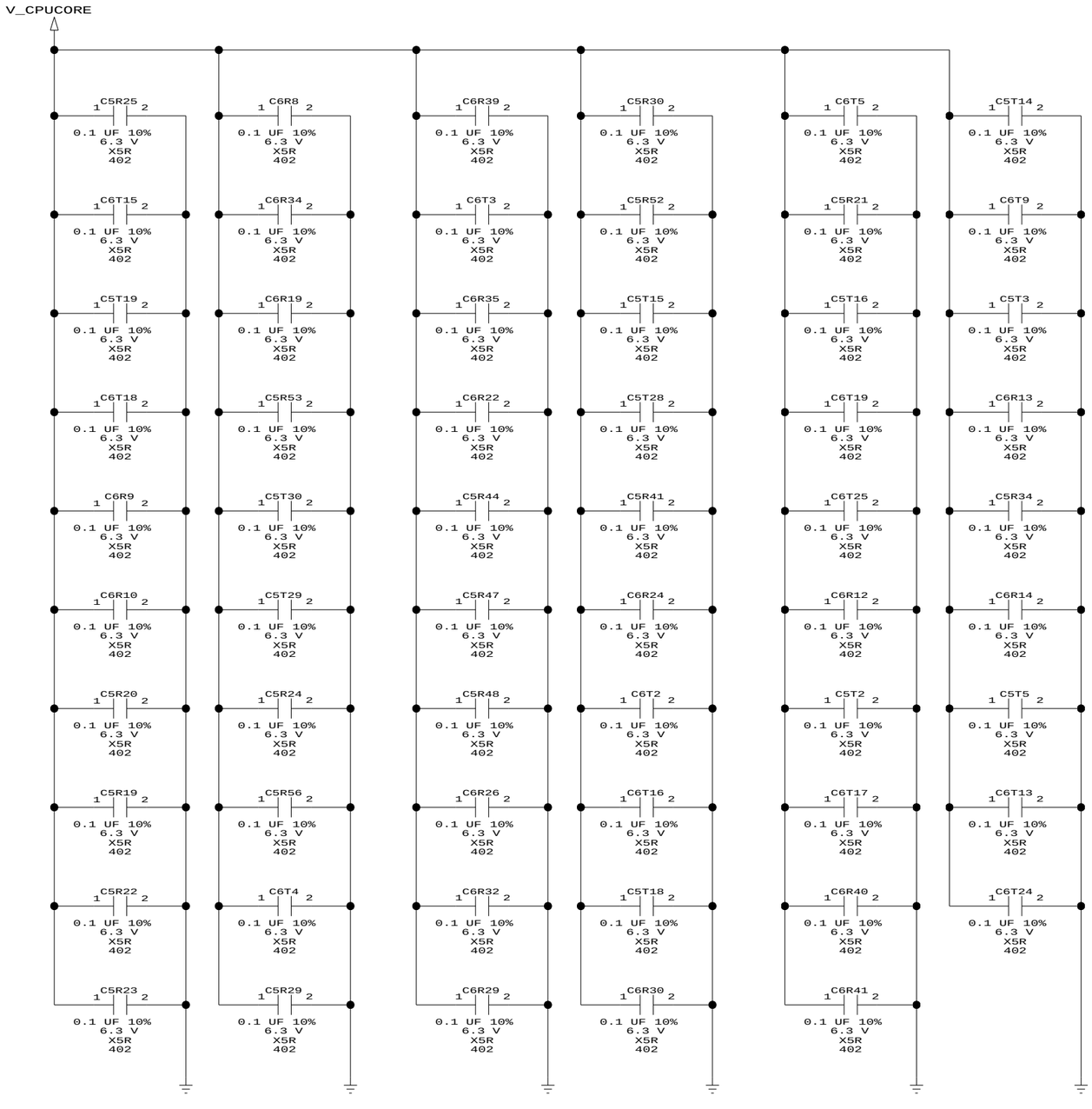


[PAGE_TITLE=GCPU, DECOUPLING]

DRAWING
Fri Jan 04 12:07:13 2013

MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 10/74	CSA PAGE 10/74	FAB C	REV 1.0

GCPU, DECOUPLING



[PAGE_TITLE=GCPU, DECOUPLING]

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Fri Jan 04 12:07:13 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	11/74	11/74	C	1.0

GPU, MEMORY CONTROLLER 0 PARTITION A & B

U5E1 4 OF 17 IC

GCPU VERSION 1

MA_DQ31	T34	MA_DQ31	MA_CLK1_DP	AE28
MA_DQ30	T33	MA_DQ30	MA_CLK1_DN	AE30
MA_DQ29	U31	MA_DQ29	MA_CLK0_DP	AC33
MA_DQ28	R33	MA_DQ28	MA_CLK0_DN	AC34
MA_DQ27	U33	MA_DQ27		
MA_DQ26	R32	MA_DQ26	MA_A12	AL33
MA_DQ25	V33	MA_DQ25	MA_A11	AH34
MA_DQ24	R31	MA_DQ24	MA_A10	AL34
MA_WDQS3	R34	MA_WDQS3	MA_A9	AG34
MA_RDQS3	U32	MA_RDQS3	MA_A8	AD33
MA_DM3	U34	MA_DM3	MA_A7	AF34
			MA_A6	AE33
MA_DQ23	Y34	MA_DQ23	MA_A5	AD34
MA_DQ22	Y33	MA_DQ22	MA_A4	AF33
MA_DQ21	Y32	MA_DQ21	MA_A3	AG33
MA_DQ20	AA33	MA_DQ20	MA_A2	AH33
MA_DQ19	W33	MA_DQ19	MA_A1	AK33
MA_DQ18	AB31	MA_DQ18	MA_A0	AJ34
MA_DQ17	V34	MA_DQ17		
MA_DQ16	AB32	MA_DQ16	MA_BA2	AE34
MA_WDQS2	AA34	MA_WDQS2	MA_BA1	AE32
MA_RDQS2	Y31	MA_RDQS2	MA_BA0	AK34
MA_DM2	W34	MA_DM2		
MA_DQ15	W28	MA_DQ15	MA_CKE	AJ33
MA_DQ14	R30	MA_DQ14	MA_WE_N*	AF29
MA_DQ13	W30	MA_DQ13	MA_CAS_N*	AG30
MA_DQ12	R28	MA_DQ12	MA_RAS_N*	AH30
MA_DQ11	V28	MA_DQ11	MA_CS1_N*	AF30
MA_DQ10	T29	MA_DQ10	MA_CS0_N*	AE31
MA_DQ9	U29	MA_DQ9		
MA_DQ8	U28	MA_DQ8		
MA_WDQS1	T30	MA_WDQS1		
MA_RDQS1	V30	MA_RDQS1		
MA_DM1	V32	MA_DM1		
MA_DQ7	Y30	MA_DQ7		
MA_DQ6	AD28	MA_DQ6		
MA_DQ5	Y28	MA_DQ5		
MA_DQ4	AD30	MA_DQ4		
MA_DQ3	AB28	MA_DQ3		
MA_DQ2	AC30	MA_DQ2		
MA_DQ1	AB29	MA_DQ1		
MA_DQ0	AC28	MA_DQ0		
MA_WDQS0	AC32	MA_WDQS0		
MA_RDQS0	AA29	MA_RDQS0		
MA_DM0	AA30	MA_DM0		
MA_VREF0	AB34			

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MA_A<11..0> → 14 15

MA_BA<2..0> → 14 15

MA_CLK1_DP, MA_CLK1_DN → 15; MA_CLK0_DP, MA_CLK0_DN → 14

MA_CKE, MA_WE_N*, MA_CAS_N*, MA_RAS_N*, MA_CS1_N* → 14 15; MA_CS0_N* → 14

MA_WDQS1 — R6T8 4.75 KOHM 1% 402 CH — MA_DQ12

MA_DQ4 — R6T7 4.75 KOHM 1% 402 CH — MA_WDQS0

V_MEM

R6T5 549 OHM 1% — EMPTY 402

MA_VREF0

R6T4 1.27 KOHM 1% — EMPTY 402

NEED NEW VREF RESISTORS

MEMORY CONTROLLER A, DECOUPLING

C6T27 0.1 UF 10% 6.3 V X5R 402

C6T10 0.1 UF 10% 6.3 V X5R 402

C6T32 0.1 UF 10% 6.3 V X5R 402

C6T29 0.1 UF 10% 6.3 V X5R 402

U5E1 3 OF 17 IC

GCPU VERSION 1

MB_DQ31	H33	MB_DQ31	MB_CLK1_DP	B32
MB_DQ30	G34	MB_DQ30	MB_CLK1_DN	A32
MB_DQ29	H34	MB_DQ29	MB_CLK0_DP	B31
MB_DQ28	F34	MB_DQ28	MB_CLK0_DN	A31
MB_DQ27	K31	MB_DQ27		
MB_DQ26	D34	MB_DQ26	MB_A12	C30
MB_DQ25	K32	MB_DQ25	MB_A11	F25
MB_DQ24	C34	MB_DQ24	MB_A10	A25
MB_WDQS3	E34	MB_WDQS3	MB_A9	E29
MB_RDQS3	J33	MB_RDQS3	MB_A8	B30
MB_DM3	J34	MB_DM3	MB_A7	B29
			MB_A6	A30
MB_DQ23	M32	MB_DQ23	MB_A5	C32
MB_DQ22	M34	MB_DQ22	MB_A4	A29
MB_DQ21	M31	MB_DQ21	MB_A3	E25
MB_DQ20	M33	MB_DQ20	MB_A2	G26
MB_DQ19	K33	MB_DQ19	MB_A1	B25
MB_DQ18	N34	MB_DQ18	MB_A0	F26
MB_DQ17	K34	MB_DQ17		
MB_DQ16	P33	MB_DQ16	MB_BA2	E28
MB_WDQS2	N33	MB_WDQS2	MB_BA1	B28
MB_RDQS2	L34	MB_RDQS2	MB_BA0	E27
MB_DM2	L33	MB_DM2		
MB_DQ15	J28	MB_DQ15	MB_CKE	A27
MB_DQ14	C33	MB_DQ14	MB_WE_N*	B26
MB_DQ13	J30	MB_DQ13	MB_CAS_N*	C26
MB_DQ12	D33	MB_DQ12	MB_RAS_N*	D26
MB_DQ11	F33	MB_DQ11	MB_CS1_N*	A28
MB_DQ10	E33	MB_DQ10	MB_CS0_N*	A26
MB_DQ9	G30	MB_DQ9		
MB_DQ8	F30	MB_DQ8		
MB_WDQS1	E30	MB_WDQS1		
MB_RDQS1	G33	MB_RDQS1		
MB_DM1	H30	MB_DM1		
MB_DQ7	K30	MB_DQ7		
MB_DQ6	P28	MB_DQ6		
MB_DQ5	K28	MB_DQ5		
MB_DQ4	P30	MB_DQ4		
MB_DQ3	M28	MB_DQ3		
MB_DQ2	N30	MB_DQ2		
MB_DQ1	M29	MB_DQ1		
MB_DQ0	N28	MB_DQ0		
MB_WDQS0	N32	MB_WDQS0		
MB_RDQS0	L29	MB_RDQS0		
MB_DM0	L30	MB_DM0		
MB_VREF0	P34			

X818336-001 BGA_2

MB_A<11..0> → 16 17

MB_BA<2..0> → 16 17

MB_CLK1_DP, MB_CLK1_DN → 17; MB_CLK0_DP, MB_CLK0_DN → 16

MB_CKE, MB_WE_N*, MB_CAS_N*, MB_RAS_N*, MB_CS1_N* → 16 17; MB_CS0_N* → 16

MB_WDQS1 — R6R2 4.75 KOHM 1% 402 CH — MB_DQ12

MB_DQ4 — R6R1 4.75 KOHM 1% 402 CH — MB_WDQS0

V_MEM

R6T2 549 OHM 1% — EMPTY 402

MB_VREF0

R6T1 1.27 KOHM 1% — EMPTY 402

MEMORY CONTROLLER B, DECOUPLING

C6R27 0.1 UF 10% 6.3 V X5R 402

C6R11 0.1 UF 10% 6.3 V X5R 402

C6R16 0.1 UF 10% 6.3 V X5R 402

C6T30 4.7 UF 10% 6.3 V X5R 603

C6R23 0.1 UF 10% 6.3 V X5R 402

C6R46 0.1 UF 10% 6.3 V X5R 402

TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=GPU, MEMORY CONTROLLER A + B]

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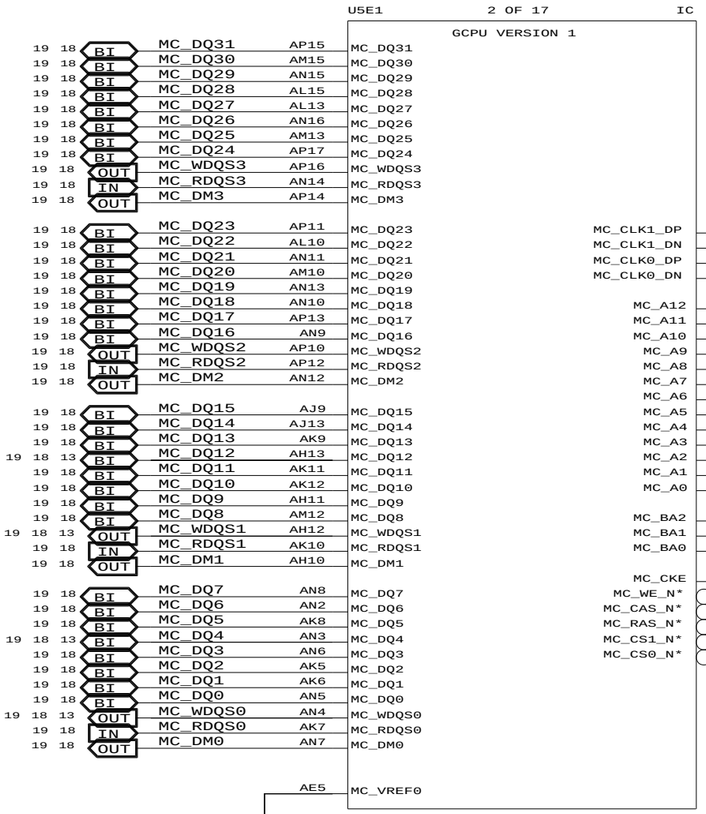
MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
CONFIDENTIAL	STINGRAY	12/74	12/74	C	1.0

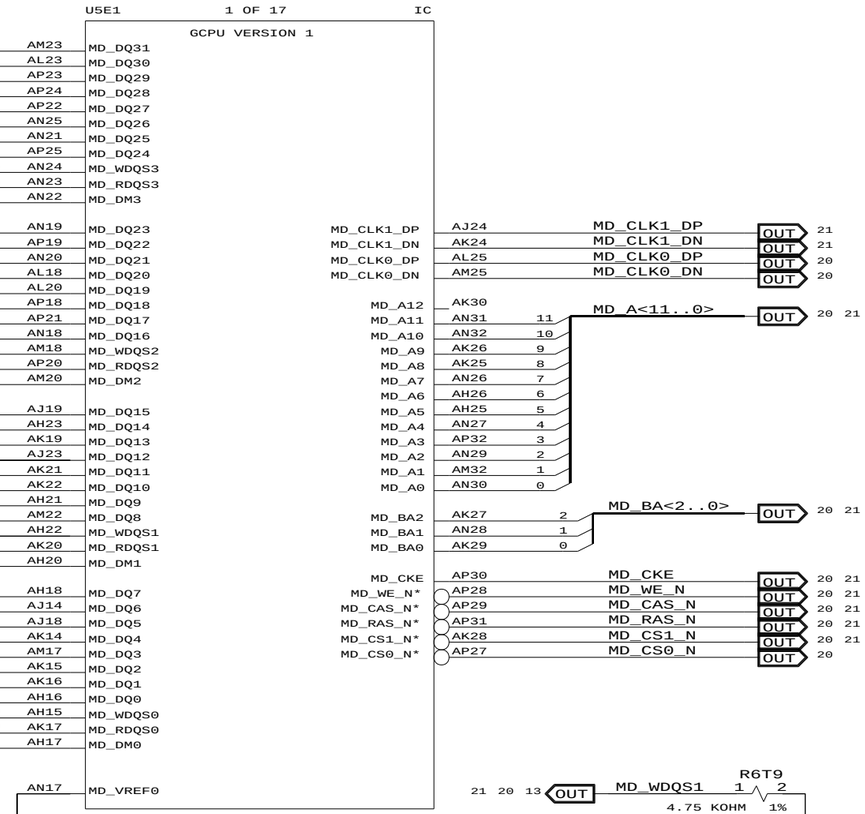
GPU, MEMORY CONTROLLER 1 PARTITION C & D



TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

GPU MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.



N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=[GPU, MEMORY CONTROLLER C + D]

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MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 13/74	CSA PAGE 13/74	FAB C	REV 1.0

MEMORY PARTITION A, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
U7E1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE
U7E1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG	PACK_IGNORE=TRUE
U7E1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND	PACK_IGNORE=TRUE

V_MEM

R7E5 60.4 OHM 1% CH 402 (1 / 2)

R7E4 60.4 OHM 1% CH 402 (1 / 2)

U7E1 — BOM_IGNORE=TRUE — EMPTY

GDDR136 (1Gbit) MF=1

12	IN	MA_CLK0_DP	J11	CLK_DP	DQ31	T3	MA_DQ31 BI 12 15
12	IN	MA_CLK0_DN	J10	CLK_DN	DQ30	T2	MA_DQ30 BI 12 15
19 18 17 16 15 4 21 20	IN	MEM_RST	V9	RESET	DQ29	R3	MA_DQ29 BI 12 15
					DQ28	R2	MA_DQ28 BI 12 15
					DQ27	M3	MA_DQ27 BI 12 15
					DQ26	N2	MA_DQ26 BI 12 15
					DQ25	L3	MA_DQ25 BI 12 15
					DQ24	M2	MA_DQ24 BI 12 15
					WDQS3	P2	MA_WDQS3 IN 12 15
					RDQS3	P3	MA_RDQS3 OUT 12 15
					DM3	N3	MA_DM3 IN 12 15
			J2	A12 (1Gbit only, dual-load)			
15 12	IN	MA_A<11..0>	11 L4	A11/A7	DQ23	T10	MA_DQ23 BI 12 15
			10 K2	A10/A8	DQ22	T11	MA_DQ22 BI 12 15
			9 M9	A9/A3	DQ21	R10	MA_DQ21 BI 12 15
			8 K11	A8/A10	DQ20	R11	MA_DQ20 BI 12 15
			7 L9	A7/A11	DQ19	M10	MA_DQ19 BI 12 15
			6 K10	A6/A2	DQ18	N11	MA_DQ18 BI 12 15
			5 H11	A5/A1	DQ17	L10	MA_DQ17 BI 12 15
			4 K9	A4/A0	DQ16	M11	MA_DQ16 BI 12 15
			3 M4	A3/A9	WDQS2	P11	MA_WDQS2 IN 12 15
			2 K3	A2/A6	RDQS2	P10	MA_RDQS2 OUT 12 15
			1 H2	A1/A5	DM2	N10	MA_DM2 IN 12 15
			0 K4	A0/A4			
					DQ15	G10	MA_DQ15 BI 12 15
15 12	IN	MA_BA<2..0>	2 H10	BA2/RAS_N	DQ14	F11	MA_DQ14 BI 12 15
			1 G9	BA1/BA0	DQ13	F10	MA_DQ13 BI 12 15
			0 G4	BA0/BA1	DQ12	E11	MA_DQ12 BI 12 15
					DQ11	C10	MA_DQ11 BI 12 15
					DQ10	C11	MA_DQ10 BI 12 15
15 12	IN	MA_CKE	H4	CKE/WE_N	DQ9	B10	MA_DQ9 BI 12 15
15 12	IN	MA_WE_N	H9	WE_N/CKE	DQ8	B11	MA_DQ8 BI 12 15
15 12	IN	MA_CAS_N	F4	CAS_N/CS_N	WDQS1	D11	MA_WDQS1 IN 12 15
15 12	IN	MA_RAS_N	H3	RAS_N/BA2	RDQS1	D10	MA_RDQS1 OUT 12 15
12	IN	MA_CS0_N	F9	CS_N/CAS_N	DM1	E10	MA_DM1 IN 12 15
15 12	IN	MA_CS1_N	J3	CS1_N (1Gbit only, single-load)			
20 18 16 4	IN	MEM_SCAN_TOP_EN	A9	MF			
					DQ7	G3	MA_DQ7 BI 12 15
19 18 17 16 15 4 21 20	IN	MEM_SCAN_EN	V4	SCAN_EN	DQ6	F2	MA_DQ6 BI 12 15
					DQ5	F3	MA_DQ5 BI 12 15
					DQ4	E2	MA_DQ4 BI 12 15
					DQ3	C3	MA_DQ3 BI 12 15
					DQ2	C2	MA_DQ2 BI 12 15
					DQ1	B3	MA_DQ1 BI 12 15
					DQ0	B2	MA_DQ0 BI 12 15
					WDQS0	D2	MA_WDQS0 IN 12 15
					RDQS0	D3	MA_RDQS0 OUT 12 15
					DM0	E3	MA_DM0 IN 12 15
15 14	IN	MEM_A_VREF1	H1	VREF1			
15	IN	MEM_A_VREF0	H12	VREF0			
					ZQ	A4	MA_ZQ_TOP

X802980-019

R7E8 243 OHM 1% CH 402 (1 / 2)

V_MEM

U7E1 — EMPTY

GDDR136 (1Gbit) MF=0

V1	VDDQ<21>	VSSQ<19>	T12
R12	VDDQ<20>	VSSQ<18>	T9
R9	VDDQ<19>	VSSQ<17>	T4
R4	VDDQ<18>	VSSQ<16>	T1
R1	VDDQ<17>	VSSQ<15>	P12
N12	VDDQ<16>	VSSQ<14>	P9
N9	VDDQ<15>	VSSQ<13>	P4
V12	VDDQ<14>	VSSQ<12>	P1
N4	VDDQ<13>	VSSQ<11>	L11
N1	VDDQ<12>	VSSQ<10>	L2
J9	VDDQ<11>	VSSQ<9>	G11
J4	VDDQ<10>	VSSQ<8>	G2
E12	VDDQ<9>	VSSQ<7>	D12
E9	VDDQ<8>	VSSQ<6>	D9
E4	VDDQ<7>	VSSQ<5>	D4
E1	VDDQ<6>	VSSQ<4>	D1
C12	VDDQ<5>	VSSQ<3>	B12
C9	VDDQ<4>	VSSQ<2>	B9
C4	VDDQ<3>	VSSQ<1>	B4
C1	VDDQ<2>	VSSQ<0>	B1
A12	VDDQ<1>		
A1	VDDQ<0>		
V2	VDD<7>	VSS<7>	V3
M12	VDD<6>	VSS<6>	L12
M1	VDD<5>	VSS<5>	L1
V11	VDD<4>	VSS<4>	G12
F12	VDD<3>	VSS<3>	G1
F1	VDD<2>	VSS<2>	A10
A11	VDD<1>	VSS<1>	V10
A2	VDD<0>	VSS<0>	A3
K12	VDDA<1>		
K1	VDDA<0>		
J12	VSSA<1>		
J1	VSSA<0>		

X802980-019

MX_CS1_N CONNECTED TO J3 TO SUPPORT 1G RAM CONFIGS.

V_MEM

R7T5 549 OHM 1% CH 402 (1 / 2)

MEM_A_VREF1 — OUT 14 15

GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND

R7T4 1.27 KOHM 1% CH 402 (1 / 2)

C7T7 0.1 UF 10% 6.3 V X5R 402

TO CHANGE MEM VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R7T4, R7E7, R7R4, R7D5, R5U4, R5F2, R6U4, R6F2

MEM VREF	RESISTOR VALUE
69%	1.21KOHM
70%	1.27KOHM
72%	1.40KOHM

THESE ARE THE MEM VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R7T4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE

PARTITION A DECOUPLING

V_MEM

C7E8 4.7 UF 10% 6.3 V X5R 603 (1 / 2)

MEMORY A, TOP, DECOUPLING

V_MEM

C7E14	C7E11	C7E6	C7E5	C7E13	C7E10	C7E4	C7E7
0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402	0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION A, TOP]

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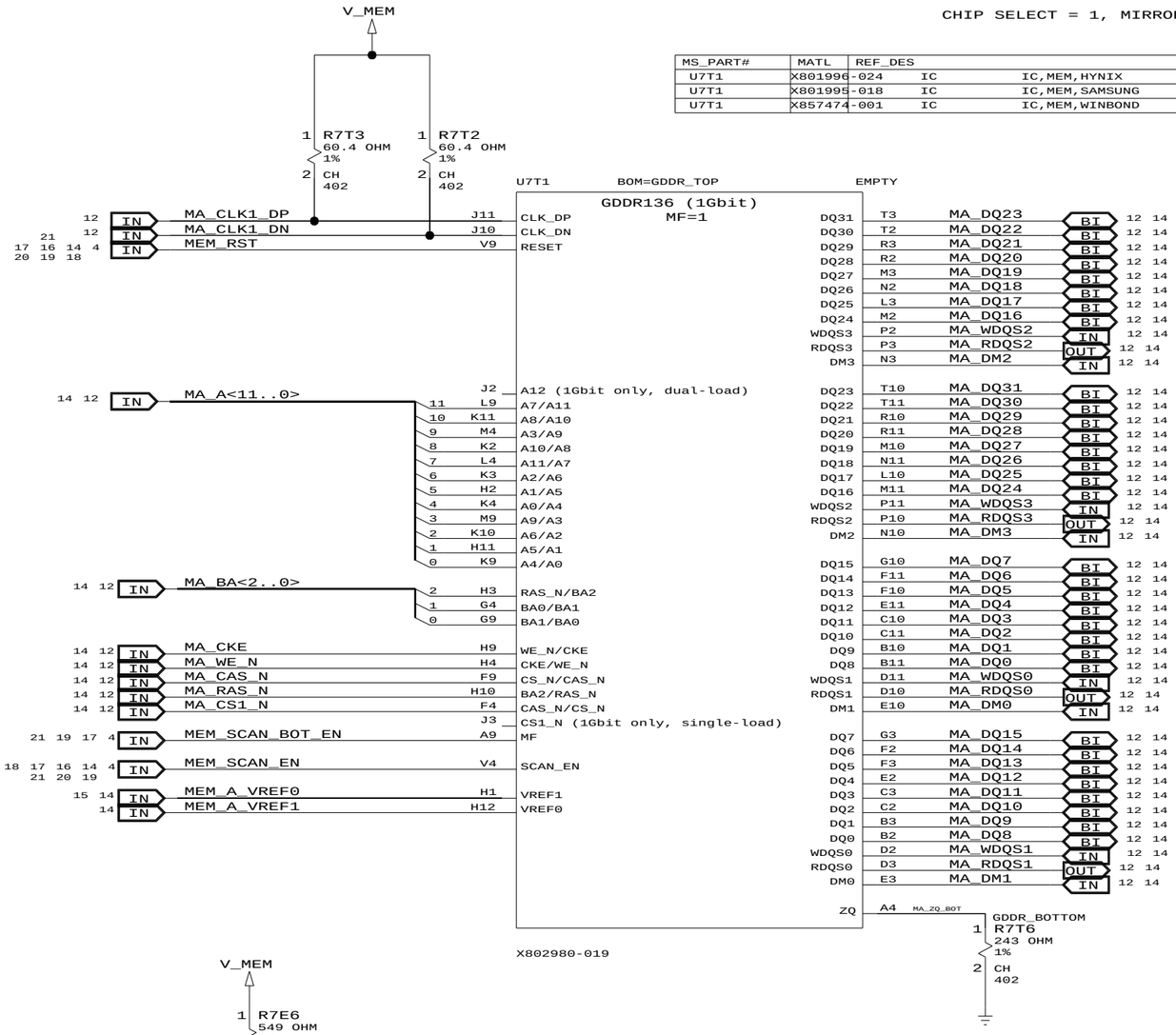
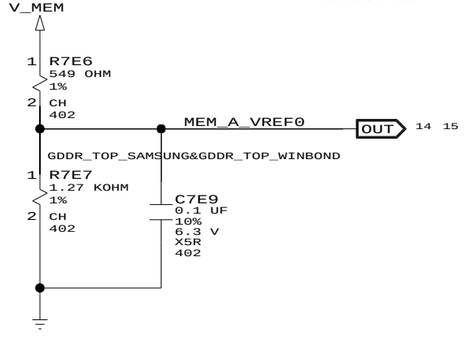
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 14/74	CSA PAGE 14/74	FAB C	REV 1.0

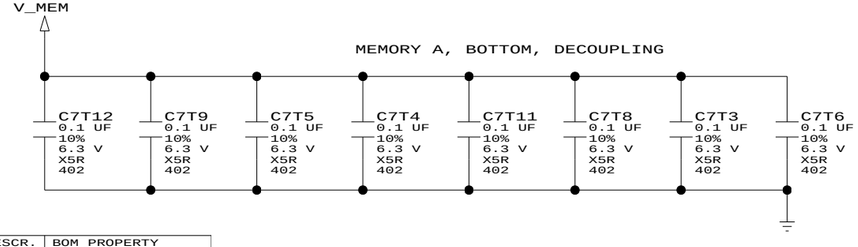
MEMORY PARTITION A, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
U7T1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX	PACK_IGNORE=TRUE
U7T1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG	PACK_IGNORE=TRUE
U7T1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND	PACK_IGNORE=TRUE







MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R7E7	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE

[PAGE_TITLE=MEMORY PARTITION A, BOTTOM]

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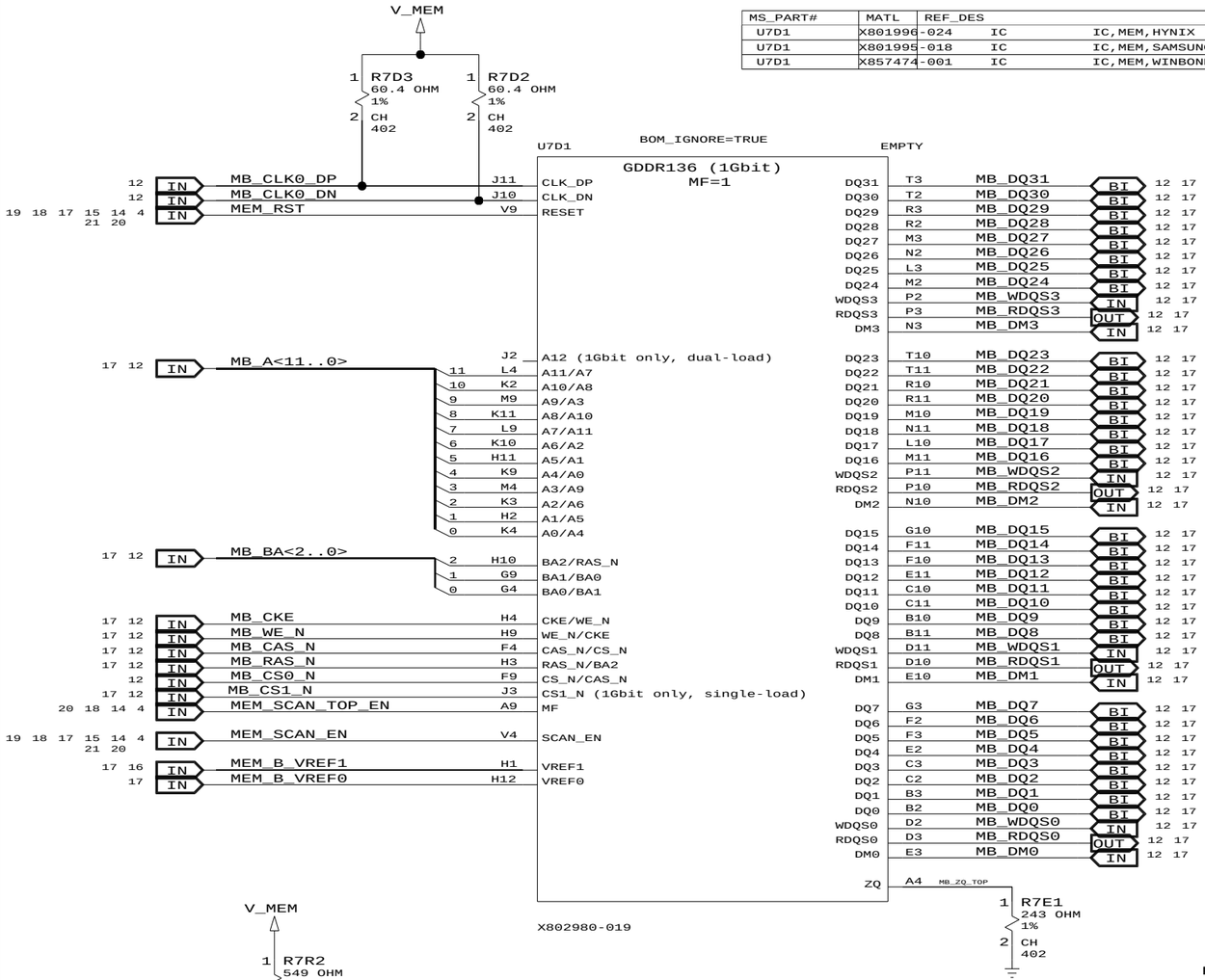
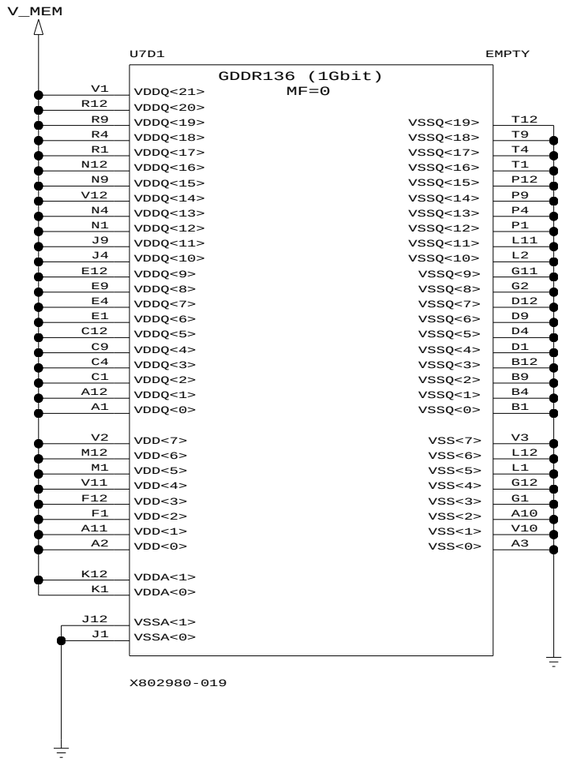
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 15/74	CSA PAGE 15/74	FAB C	REV 1.0

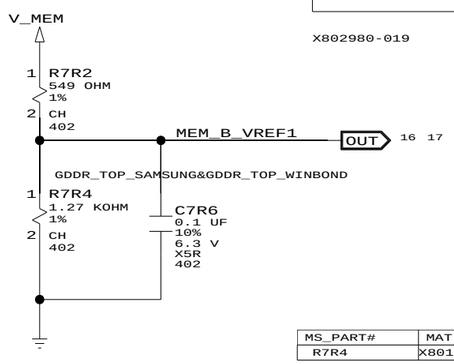
MEMORY PARTITION B, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
U7D1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX PACK_IGNORE=TRUE
U7D1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG PACK_IGNORE=TRUE
U7D1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND PACK_IGNORE=TRUE

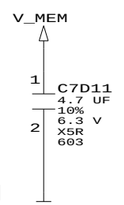


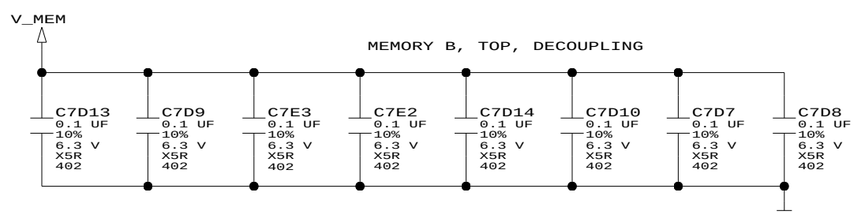




MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
R7R4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE

PARTITION B DECOUPLING





[PAGE_TITLE=MEMORY PARITION B, TOP]

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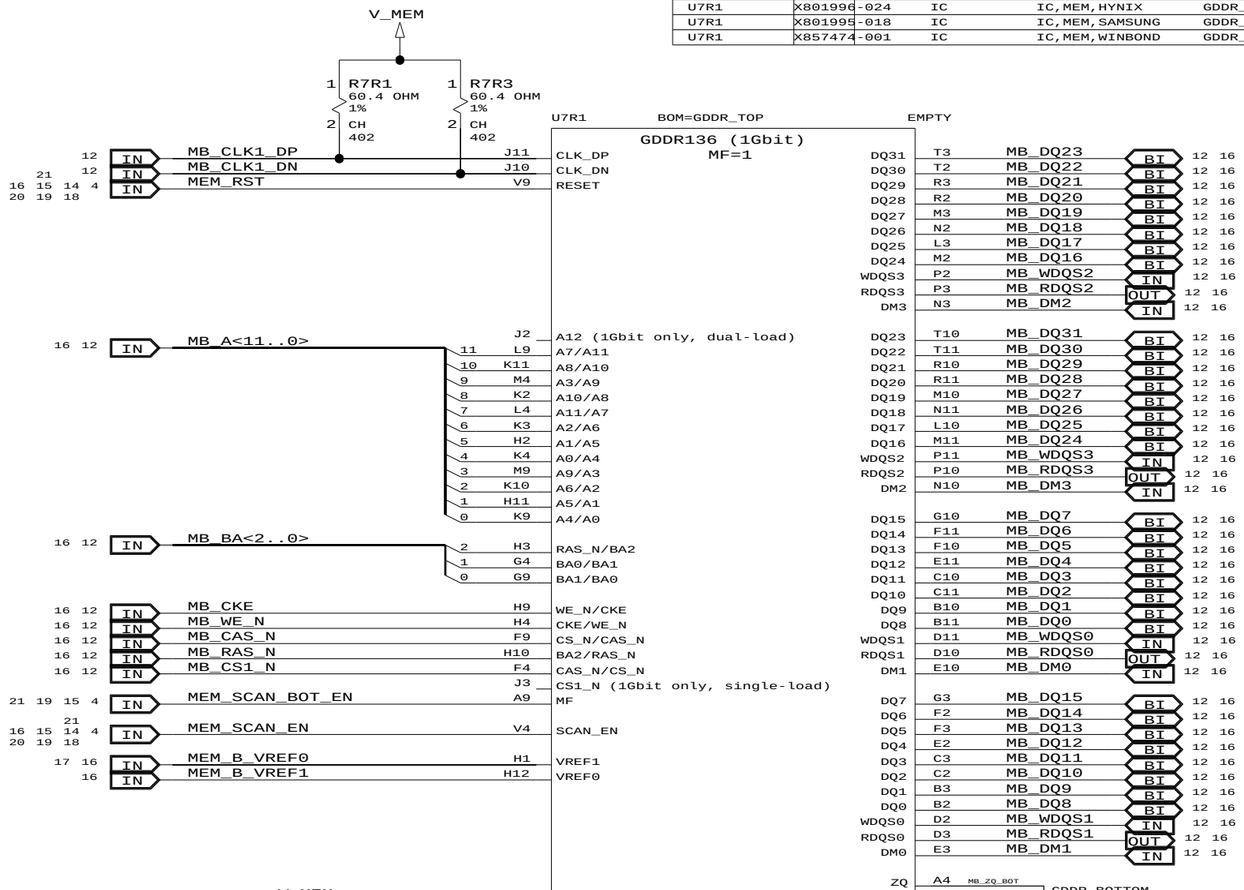
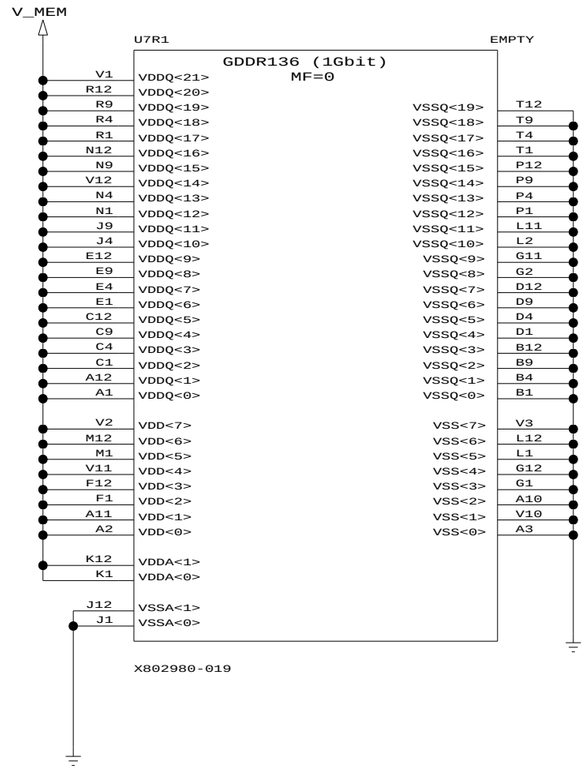
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 16/74	CSA PAGE 16/74	FAB C	REV 1.0

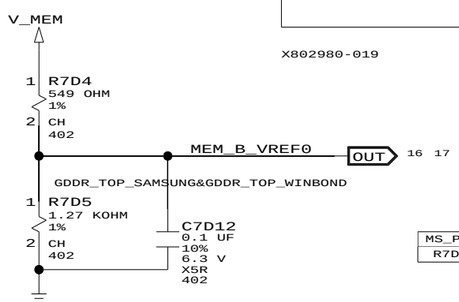
MEMORY PARTITION B, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

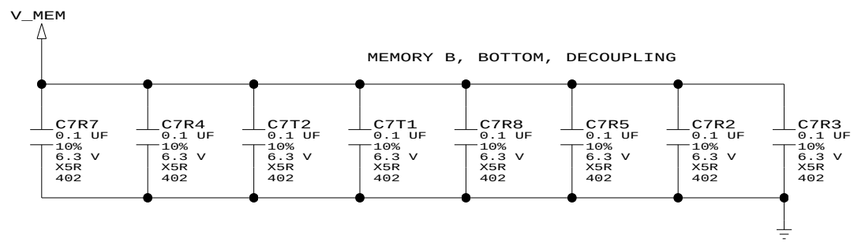
MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
U7R1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX	PACK_IGNORE=TRUE
U7R1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG	PACK_IGNORE=TRUE
U7R1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND	PACK_IGNORE=TRUE







MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R7D5	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE



[PAGE_TITLE=MEMORY PARITION B, BOTTOM]

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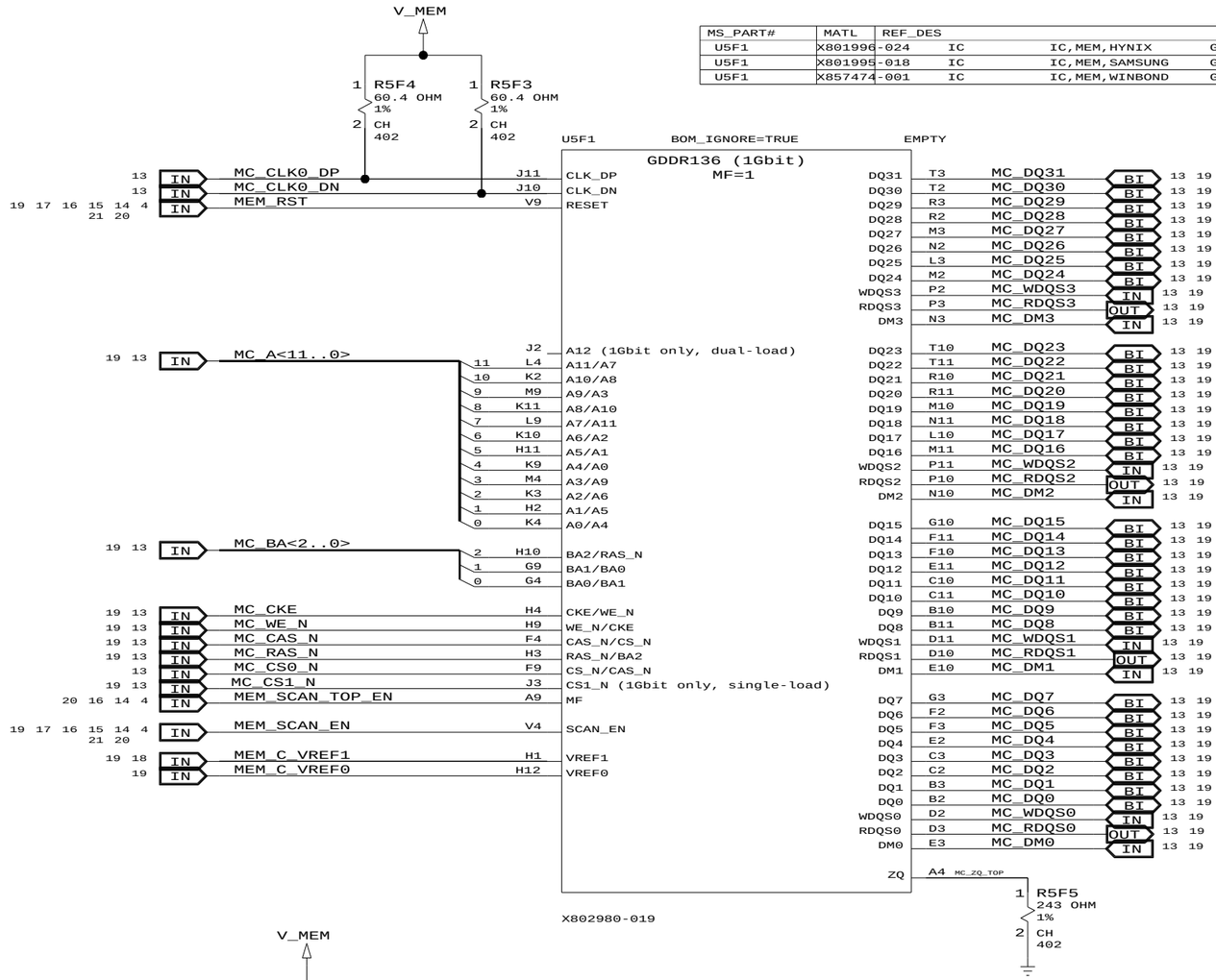
Fri Jan 04 12:07:15 2008

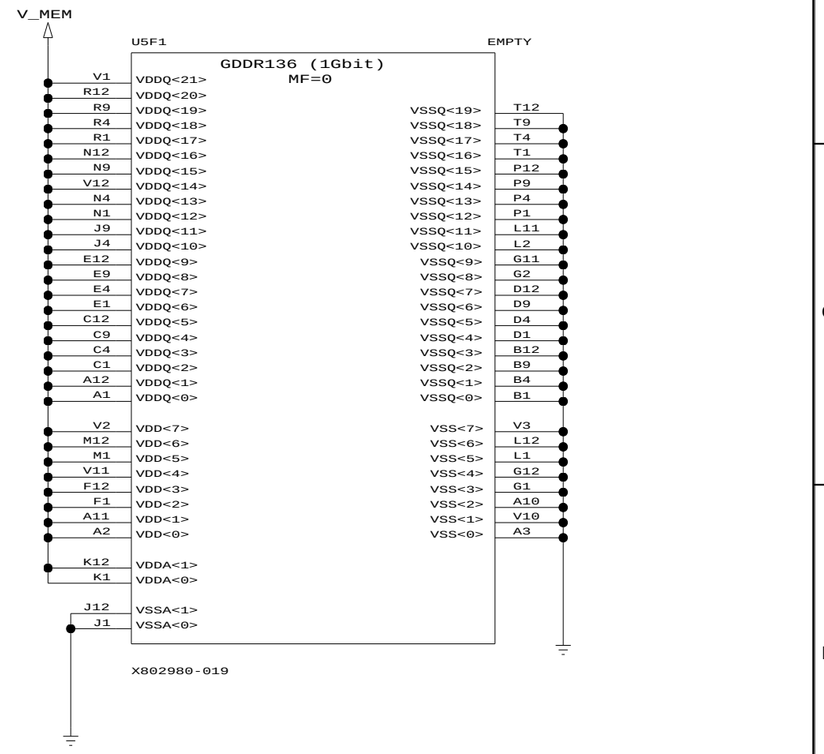
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	17/74	17/74	C	1.0

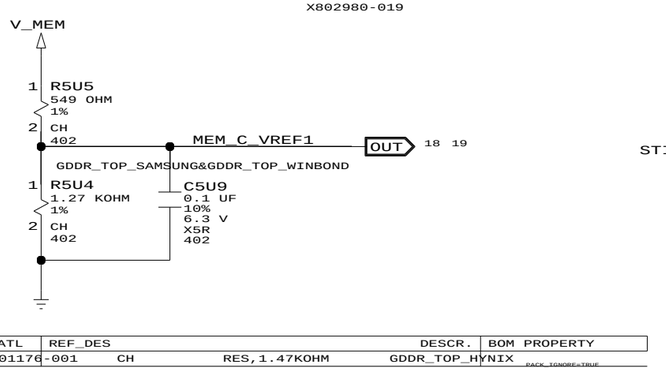
MEMORY PARTITION C, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
U5F1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE
U5F1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG	PACK_IGNORE=TRUE
U5F1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND	PACK_IGNORE=TRUE

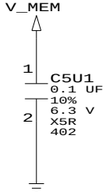




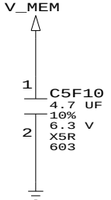


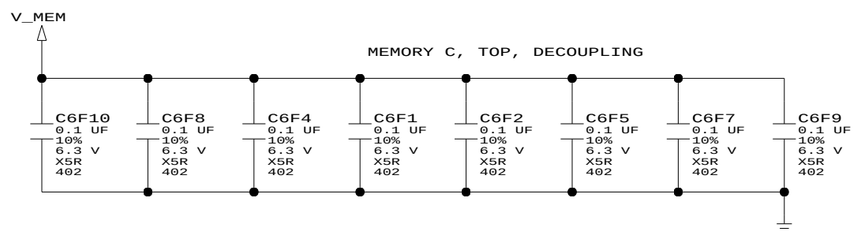
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
R5U4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE

MC_CLK0
STITCHING CAP



PARTITION C DECOUPLING





[PAGE_TITLE=MEMORY PARTITION C, TOP]

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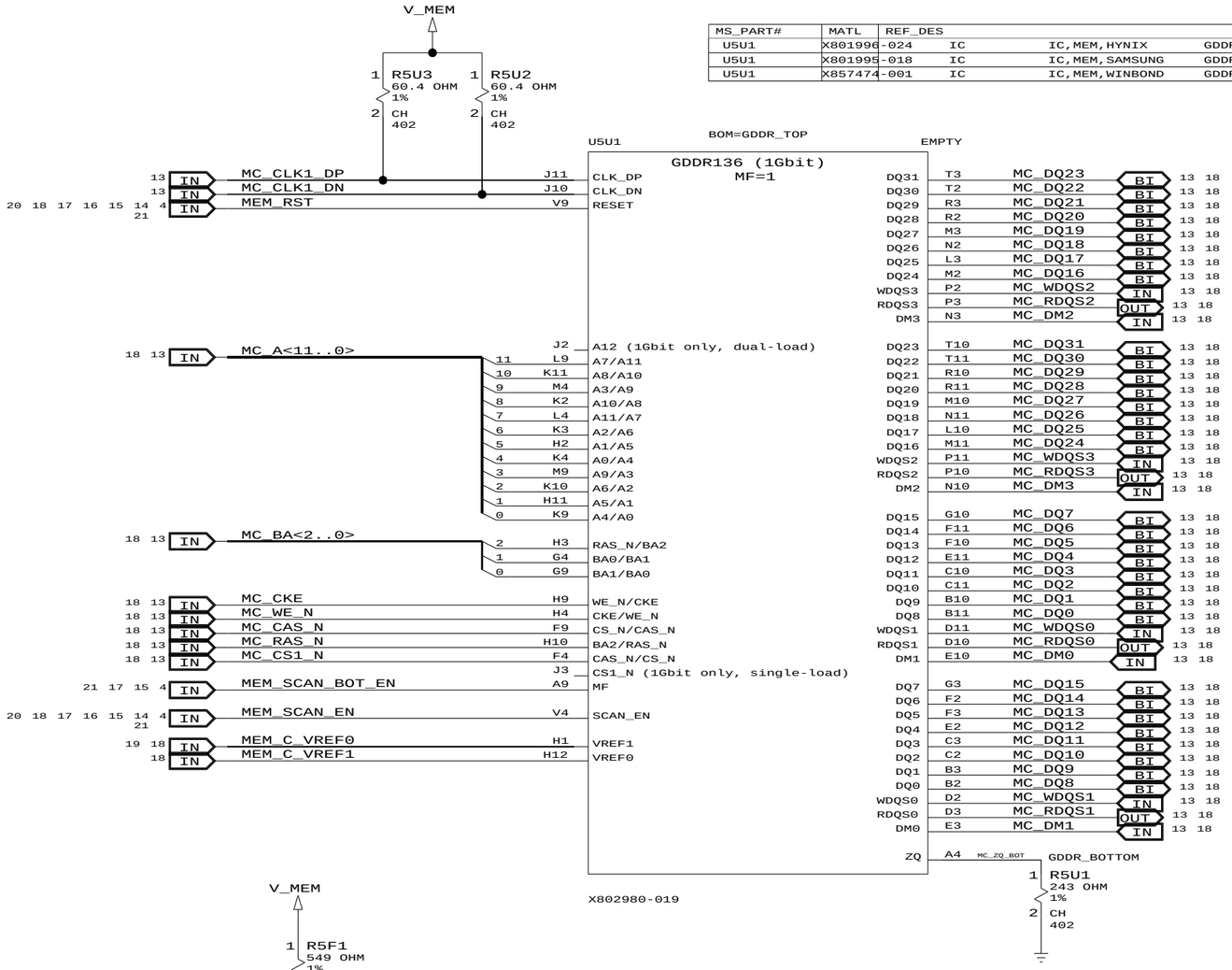
Fri Jan 04 12:07:15 2008

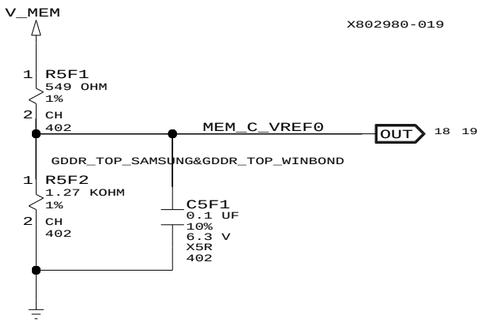
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	18/74	18/74	C	1.0

MEMORY PARTITION C, BOTTOM

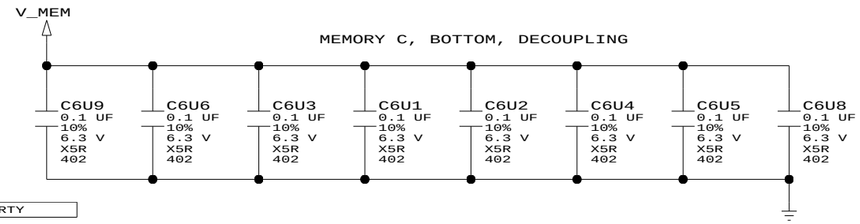
CHIP SELECT = 1, MIRROR FUNCTION = 1

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
U5U1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX PACK_IGNORE=TRUE
U5U1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG PACK_IGNORE=TRUE
U5U1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND PACK_IGNORE=TRUE





MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
R5F2	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE



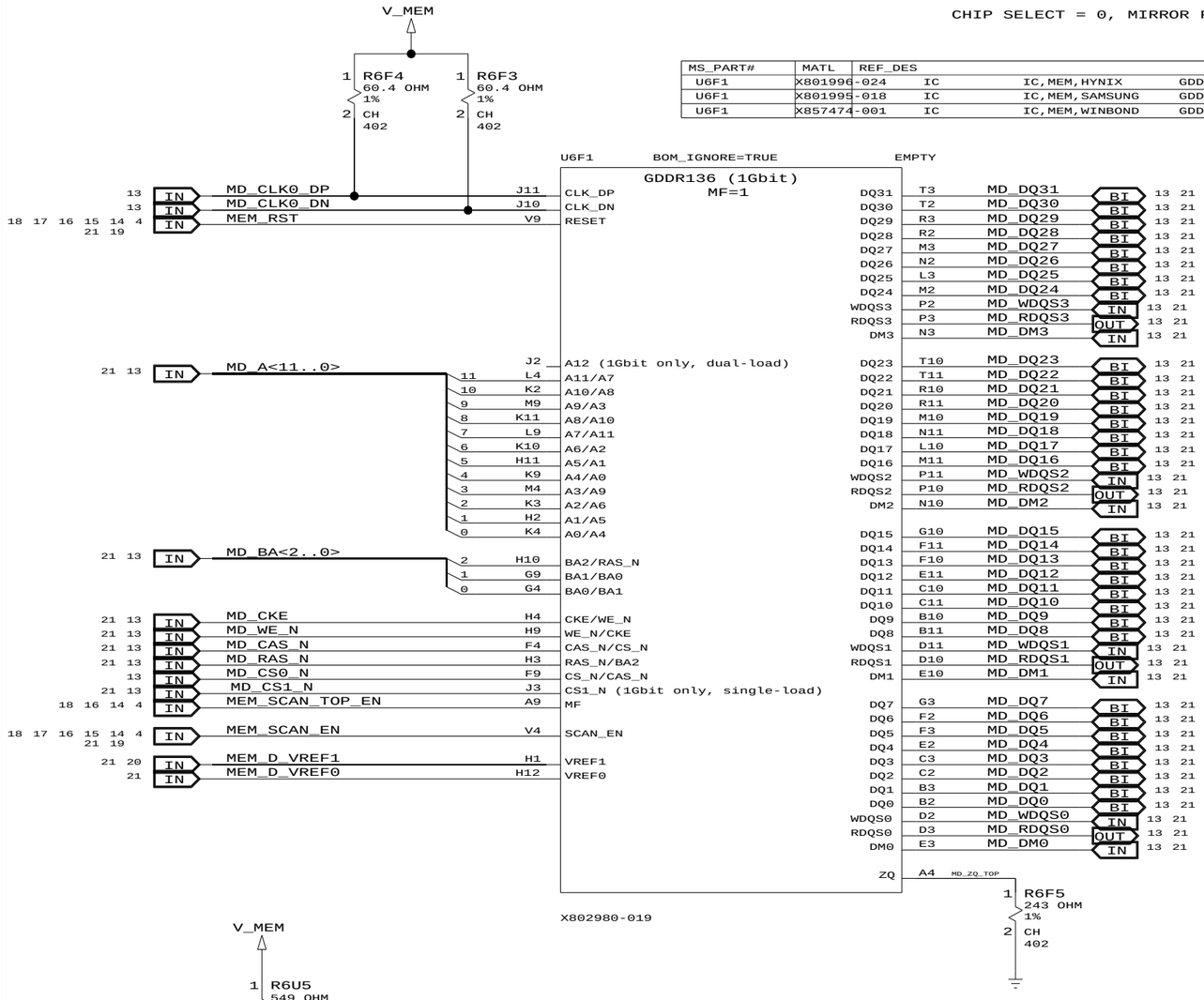
[PAGE_TITLE=MEMORY PARITION C, BOTTOM]

DRAWING
Fri Jan 04 12:07:15 2008

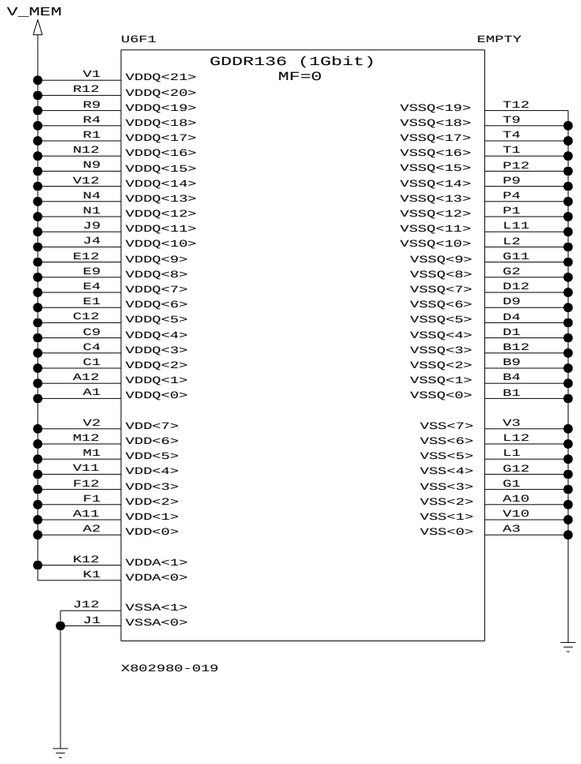
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 19/74	CSA PAGE 19/74	FAB C	REV 1.0

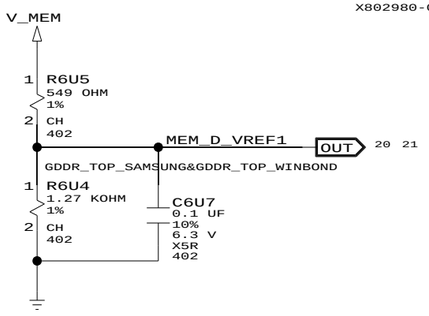
MEMORY PARTITION D, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0



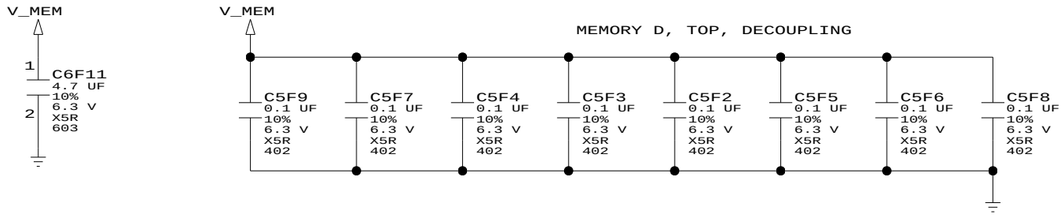
MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
U6F1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE
U6F1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG	PACK_IGNORE=TRUE
U6F1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND	PACK_IGNORE=TRUE





MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R6U4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX	PACK_IGNORE=TRUE

PARTITION D DECOUPLING



[PAGE_TITLE=MEMORY PARTITION D, TOP]

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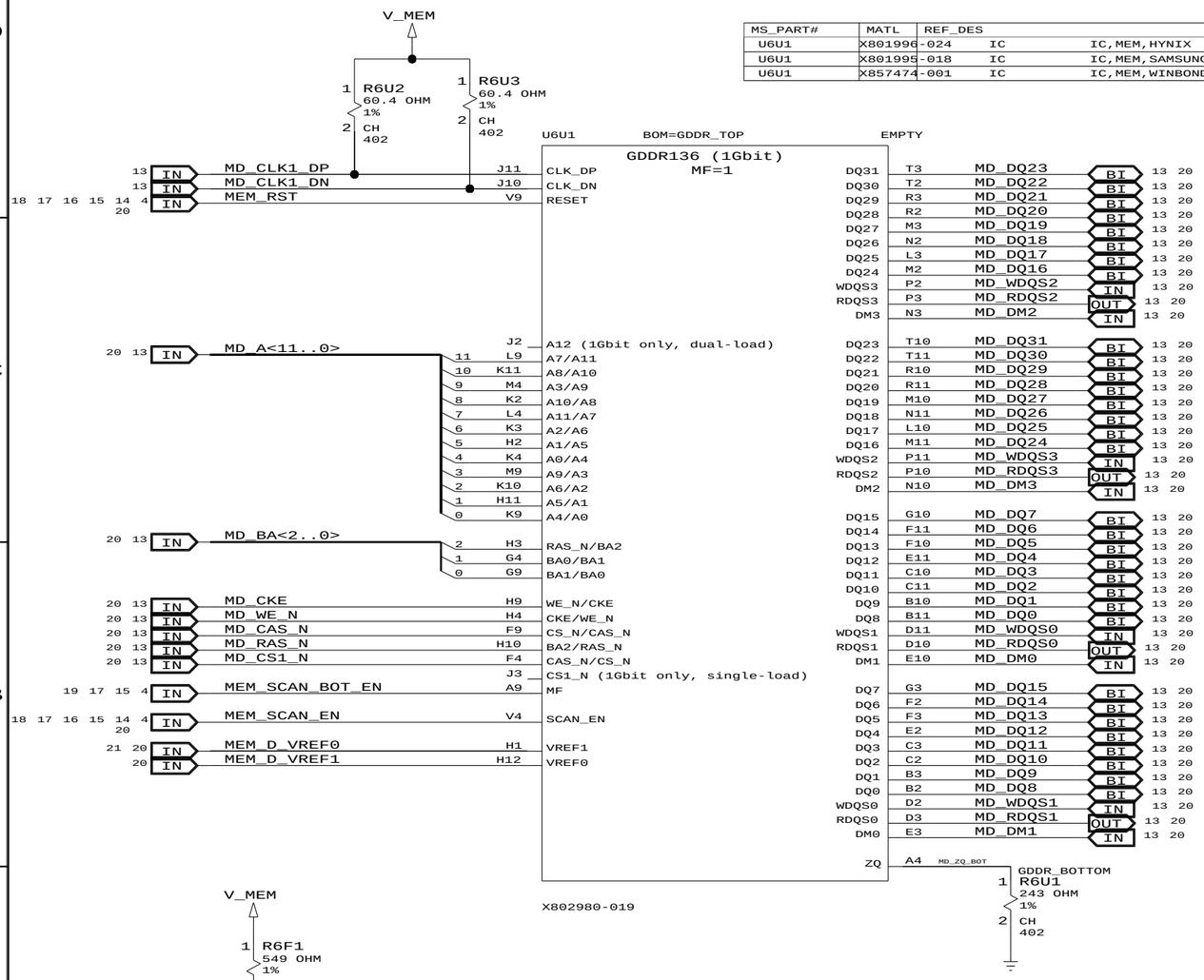
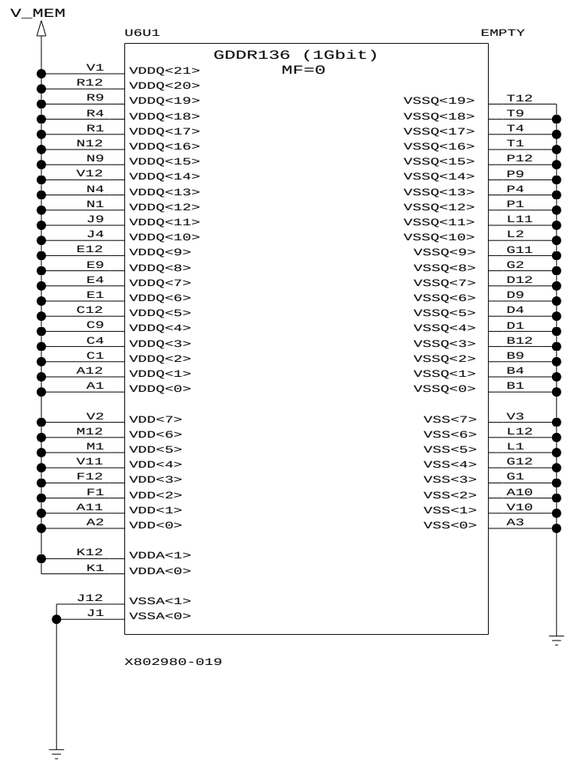
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	20/74	20/74	C	1.0

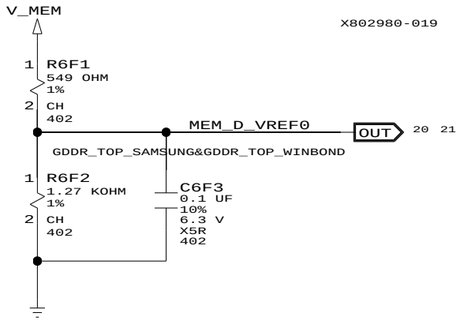
MEMORY PARTITION D, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

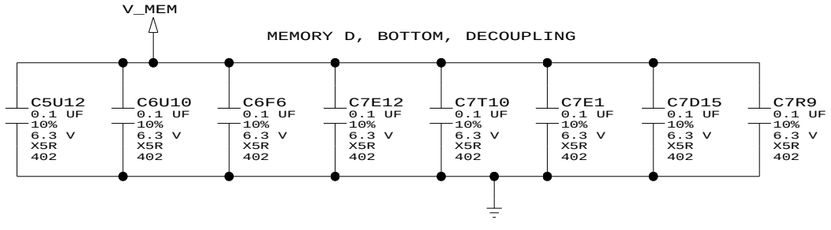
MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
U6U1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX PACK_IGNORE=TRUE
U6U1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG PACK_IGNORE=TRUE
U6U1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND PACK_IGNORE=TRUE

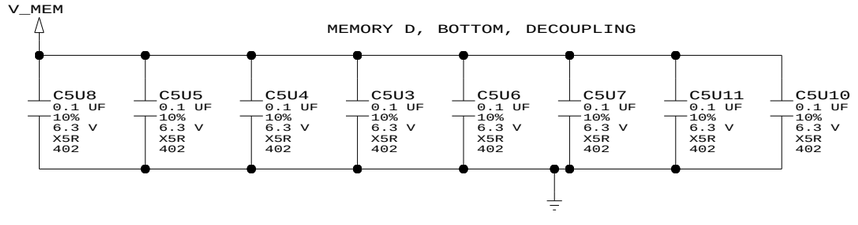






MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
R6F2	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE





[PAGE_TITLE=MEMORY PARTITION D, BOTTOM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	21/74	21/74	C	1.0

KSB, CLOCKS + STRAPPING + POR

XTAL BYPASS: STUFF R3, R4, R5, AND C153 AND
APPLY SQUARE WAVE TO XTAL_IN (VL=0V VH=1V)
KEEP R5 CLOSE TO KSB CHIP

RESISTOR VALUES CHOSEN TO GIVE V_12P0_DET 1P8V NOMINAL

V_12P0
R3R5 1% 84.5 KOHM CH 402
R3R17 1% 15 KOHM CH 402
C3R55 470 PF 5% 50 V EMPTY 402
DB3D2
Y3D1 25 MHZ SM XTAL
C3D7 27 PF 5% 50 V COG 402
C3D8 22 PF 5% 50 V NPO 402
R3D26 49.9 OHM 1% EMPTY 402
V_3P3STBY
R3D17 8.25 KOHM 1% EMPTY 402
R3D19 1.5 KOHM 1% EMPTY 402
C3D1 0.01 UF 10% 16 V EMPTY 402

U3D1 KSB IC
1 OF 9
X850744-001 PBGA404 I155

V_12P0_OK	C5	
V_RST_OK<DN>	V19	
V_12P0_DET	W20	V_12P0_DET
POR_BYPASS	B4	POR_BYPASS<DN>
MAIN_PWR_OK	C4	
SB_RST_N*	C9	SB_RST_N_R
SMC_RST_N_OUT	D7	SMC_RST_N_R
XTAL_IN	AB21	XTAL_IN
CPU_CLK_DP	U21	CPU_CLK_DP_R
CPU_CLK_DN	V21	CPU_CLK_DN_R
NB_CLK_DP	V22	GPU_CLK_DP_R
NB_CLK_DN	W22	GPU_CLK_DN_R
XTAL_OUT	AA21	XTAL_OUT
XTAL_VSS	AA22	
PCIEX_CLK_IN_DP	Y15	EXT_PCIEX_CLK_DP
PCIEX_CLK_IN_DN	AA15	EXT_PCIEX_CLK_DN
PIX_CLK_OUT_DP	U22	PIX_CLK_2X_DP_R
PIX_CLK_OUT_DP	T22	PIX_CLK_2X_DN_R
EXT_CLK48_IN	Y20	CLK48<DN>
EXT_CLK48_SEL	W19	CLK48_BYPASS<DN>
SMB_DATA	A4	SMB_DATA
SMB_CLK	A5	SMB_CLK

DB2C2 POR_BYPASS
DB3D3 EXT_CLK48_IN
DB3D1 EXT_CLK48_SEL
62 61 55 25 BI SMB_DATA
62 61 55 25 BI SMB_CLK

SB_KSB_BASE
V12P0_PWRGD → OUT 25 42 → FTP FT2P6
V_RST_OK → OUT → FTP FT3R3
SB_MAIN_PWRGD ← IN 25 ← FTP FT3P5
R3P2 1 KOHM 5% CH 402
SB_RST_N ← IN 25
R2P3 10 KOHM 5% CH 402
R3P15 10 KOHM 5% CH 402
R3P16 1 KOHM 5% CH 402
SMC_RST_N → OUT 25 42 62
R3D6 33 OHM 5% 402 CH
R3D7 49.9 OHM 1% 402 CH
CPU_CLK_DP → OUT 2
CPU_CLK_DN → OUT 2
R3D8 33 OHM 5% 402 CH
R3D9 49.9 OHM 1% 402 CH
R3D10 33 OHM 5% 402 CH
R3D11 49.9 OHM 1% 402 CH
GPU_CLK_DP → OUT 4
GPU_CLK_DN → OUT 4
R3D12 33 OHM 5% 402 CH
R3D13 49.9 OHM 1% 402 CH
V_3P3
R3D28 10 KOHM 1% CH 402
DB3R6
DB3R7
R3D29 10 KOHM 1% CH 402
R3D5 33 OHM 5% 402 CH
R3D14 60.4 OHM 1% 402 CH
PIX_CLK_2X_DP → OUT 4
PIX_CLK_2X_DN → OUT 4
R3D3 33 OHM 5% 402 CH
R3D4 60.4 OHM 1% 402 CH
FTP FT3R7
FTP FT3R2

I2C ADDRESS

	0011 100 R/W HEX		0111 000 R/W HEX
WRITE	0011 100 0	0X38	0111 000 0 0X70
READ	0011 100 1	0X39	0111 000 1 0X71

	0011 110 R/W HEX	
WRITE	0011 110 0	0X3C
READ	0011 110 1	0X3D

[PAGE_TITLE=KSB, CLOCKS + STRAPING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	22/74	22/74	C	1.0

KSB, VIDEO + FAN

U3D1 KSB IC

2 OF 9

4 IN GPU_PIX_CLK_1X — J20 PIX_CLK_IN

4 IN PIX_DATA<14..0>

14	G20	PIX_DATA14
13	G21	PIX_DATA13
12	G22	PIX_DATA12
11	H20	PIX_DATA11
10	H21	PIX_DATA10
9	H22	PIX_DATA9
8	J21	PIX_DATA8
7	J22	PIX_DATA7
6	K21	PIX_DATA6
5	K22	PIX_DATA5
4	K20	PIX_DATA4
3	L21	PIX_DATA3
2	L22	PIX_DATA2
1	L20	PIX_DATA1
0	M20	PIX_DATA0

4 IN GPU_HSYNC_OUT — M22 HSYNC_IN

4 IN GPU_VSYNC_OUT — M21 VSYNC_IN

DAC_RSET — D20 DAC_RSET

R3P11 5.11 KOHM 0.1% CH 402

DAC_RSET ROUTING SENSITIVE TO NOISE ROUTE MUST REMAIN LOCKED

61 38 IN BRD_TEMP_P — R4G2 0 OHM 5% 402 EMPTY — BRD_TEMP_P_DIODE — Q4G1 EMPTY

61 38 OUT BRD_TEMP_N — R4G1 0 OHM 5% 402 EMPTY — BRD_TEMP_N_DIODE

40 IN HDMI_HPD — D18 HDMI_HPD

KSB_RSET — H4 RSET

R2P4 2 KOHM 1% CH 402

FT3P1 FTP 1

25 IN SMC_PWM0 — R3P3 205 KOHM 1% 402 EMPTY — FAN_OP1_DP — F22 FAN_OP1_DP

C3P2 0.22 UF 10% 6.3 V EMPTY 402

36 IN FAN1_FDBK — F21 FAN_OP1_DN

P22 TEMP_N

66 61 IN CPU_TEMP_N_KSB — ST3C5 SHORT

66 61 IN GPU_TEMP_N_KSB — ST3C2 SHORT

66 61 IN EDRAM_TEMP_N_KSB — ST3C4 SHORT

61 IN BRD_TEMP_N_KSB — ST3C3 SHORT

23 IN CAL_TEMP_N — ST3C1 SHORT

X850744-001 PBGA404

DAC_D_OUT_DP	A20	VID_DACD_DP	OUT 37
DAC_D_OUT_DN	F18		
DAC_B_OUT_DP	A21	VID_DACB_DP	OUT 37
DAC_B_OUT_DN	G18		
DAC_A_OUT_DP	C22	VID_DACA_DP	OUT 37
DAC_A_OUT_DN	G19		
DAC_C_OUT_DP	D22	VID_DACC_DP	OUT 37
DAC_C_OUT_DN	H18		
HSYNC_OUT	B19	VID_HSYNC_OUT_R	OUT
VSYNC_OUT	C19	VID_VSYNC_OUT_R	OUT
TMDS_TXC_DP	A16	HDMI_TXC_DP	C3C4 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TXC_DP_R — R3C23 301 OHM 1% 603 EMPTY — OUT 40
TMDS_TXC_DN	B16	HDMI_TXC_DN	OUT 40
TMDS_TX2_DP	B13	HDMI_TX2_DP	C3C1 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX2_DP_R — R3C20 301 OHM 1% 603 EMPTY — OUT 40
TMDS_TX2_DN	C13	HDMI_TX2_DN	OUT 40
TMDS_TX1_DP	A14	HDMI_TX1_DP	C3C2 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX1_DP_R — R3C21 301 OHM 1% 603 EMPTY — OUT 40
TMDS_TX1_DN	B14	HDMI_TX1_DN	OUT
TMDS_TX0_DP	B15	HDMI_TX0_DP	C3C3 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX0_DP_R — R3C22 301 OHM 1% 603 EMPTY — OUT 40
TMDS_TX0_DN	C15	HDMI_TX0_DN	OUT 40
DDC_SCK	A12	HDMI_DDC_CLK	BI 40 55
DDC_SDA	B12	HDMI_DDC_DATA	BI 40 55
FAN_OUT1	E21	FAN1_OUT	OUT 36
TEMP3_P	N22	CAL_TEMP_P	DB3P1 DB3R1 DB3P2 DB3R2 — C3R1 100 PF 5% 50 V EMPTY 402
TEMP2_P	P20	GPU_TEMP_P_KSB	OUT 61 66
TEMP1_P	P21	CPU_TEMP_P_KSB	OUT 61 66
TEMP0_P	R21	EDRAM_TEMP_P_KSB	OUT 61 66
TEMP4_P	N21	BRD_TEMP_P_KSB	OUT 61

CAL_TEMP_N — OUT 23

CUSTOM THERMAL CALIBRATION PADS LOCATION MUST REMAIN LOCKED

[PAGE_TITLE=KSB, VIDEO + FAN]

DRAWING Fri Jan 04 12:07:17 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	23/74	23/74	C	1.0

KSB, PCIEX + SMM GPIO + JTAG

V_3P3

RETAIL

R2C14 10 KOHM 5% EMPTY 402
R2C12 10 KOHM 5% CH 402
R2C18 10 KOHM 5% EMPTY 402
R2C16 10 KOHM 5% EMPTY 402
R2C20 10 KOHM 5% EMPTY 402

DEBUG OUTPUT DISABLED = SB_GPIO<1> HIGH

0 1 2 3 5

DEVKIT

R2C13 1 KOHM 5% CH 402
R2C11 1 KOHM 5% CH 402
R2C17 1 KOHM 5% CH 402
R2C15 1 KOHM 5% CH 402
R2C19 1 KOHM 5% CH 402

SB_GPIO<0..15> BI 24 62

U3D1 KSB IC

4 OF 9

PEX_TX1_DP	AA19	PEX_SB_GPU_L1_DP_C	C3D5 0.1 UF 10% 6.3 V X5R 402	PEX_SB_GPU_L1_DP OUT 4
PEX_TX1_DN	AB19	PEX_SB_GPU_L1_DN_C	C3D6 0.1 UF 10% 6.3 V X5R 402	PEX_SB_GPU_L1_DN OUT 4
PEX_TX0_DP	AA17	PEX_SB_GPU_L0_DP_C	C3D3 0.1 UF 10% 6.3 V X5R 402	PEX_SB_GPU_L0_DP OUT 4
PEX_TX0_DN	AB17	PEX_SB_GPU_L0_DN_C	C3D4 0.1 UF 10% 6.3 V X5R 402	PEX_SB_GPU_L0_DN OUT 4
UART0_TXD	A2	KER_DBG_TXD_R	R2C9 47 OHM 5% 402 CH	KER_DBG_TXD OUT 62
TST_PT	E18	KSB_DEBUG		1 DB3P3

4 IN PEX_GPU_SB_L1_DP Y18 PEX_RX1_DP
4 IN PEX_GPU_SB_L1_DN AA18 PEX_RX1_DN
4 IN PEX_GPU_SB_L0_DP Y16 PEX_RX0_DP
4 IN PEX_GPU_SB_L0_DN AA16 PEX_RX0_DN

62 IN KER_DBG_RXD A3 UART0_RXD<UP>

V_3P3STBY

R3G19 10 KOHM 5% CH 402

62 24 IN AUD_SPI_MOSI_R — R2C21 0 OHM 5% 402 CH — AUD_SPI_MOSI OUT 35

R2C1 10 KOHM 5% EMPTY 402

V_3P3STBY

R3G18 10 KOHM 5% CH 402

62 24 OUT AUD_SPI_MISO_R — R2C25 0 OHM 5% 402 CH — AUD_SPI_MISO IN 35

R2C24 10 KOHM 5% EMPTY 402

V_3P3STBY

R3G3 10 KOHM 5% CH 402

62 24 IN AUD_SPI_CLK_R — R2C23 0 OHM 5% 402 CH — AUD_SPI_CLK OUT 35

R2C22 10 KOHM 5% EMPTY 402

V_3P3STBY

R2G6 10 KOHM 5% CH 402

62 24 IN AUD_RDY_BSBY_R — R2G5 0 OHM 5% 402 CH — AUD_RDY_BSBY OUT 35

R2G7 10 KOHM 5% EMPTY 402

GPIO<1> = 0 ENABLE DEBUG OUTPUT
1 DISABLE DEBUG OUTPUT

GPIO<0,2,3> = 111 XENON
110 ZEPHYR A
101 ZEPHYR B
100 ZEPHYR C
011 FALCON
010 JASPER
001 TRINITY
000 CORONA

GPIO15	F2	AUD_SPI_MISO_R	IN	24 62
GPIO14	F3	AUD_SSB_R	OUT	24 62
GPIO13	E1	SCART_RGB	OUT	37 62
GPIO12	E4	AUD_RST_N	OUT	33
GPIO11	E3	AUD_RDY_BSBY_R	OUT	24 62
GPIO10	F4	62 FAN_TACH_SMM_R		
GPIO9	G4	WSS_CNTL0	OUT	37 62
GPIO8	G3	WSS_CNTL1	OUT	37 62
GPIO7	D3	AUD_SPI_MOSI_R	OUT	24 62
GPIO6	D4	AUD_SPI_CLK_R	OUT	24 62
GPIO5	E2	SB_GPIO<5>	BI	24 62
GPIO4	C1	SB_GPIO<4>	OUT	24 62
GPIO3	C2	SB_GPIO<3>	OUT	24 62
GPIO2	D1	SB_GPIO<2>	OUT	24 62
GPIO1	B1	SB_GPIO<1>	BI	24 62
GPIO0	B2	SB_GPIO<0>	OUT	24 62

R2P9 5% CH 0 OHM 402 — FAN_TACH IN 25 36

65 IN SB_TCLK T19 TCK<DN>
65 OUT SB_TDO R19 TDO
65 IN SB_TDI R20 TDI<UP>
65 IN SB_TMS U19 TMS<UP>
65 IN SB_TRST N19 TRST<DN>

FT3T8 FTP
FT3T7 FTP
FT3T6 FTP
FT3T5 FTP
FT3T4 FTP

X850744-001 PBGA404

V_3P3STBY

R3G20 10 KOHM 5% CH 402

62 24 IN AUD_SSB_R — R2P5 0 OHM 5% 402 CH — AUD_SSB OUT 35

R2C26 10 KOHM 5% EMPTY 402

DEBUG BUS

NET NAME	DEBUG BUS BIT
SB_GPIO<0>	0
SB_GPIO<2>	1
SB_GPIO<3>	2
SB_GPIO<4>	3
AUD_SPI_CLK_R	4
SB_GPIO<5>	5
WSS_CNTL1	6
WSS_CNTL0	7
FAN_TACH	8
AUD_RDY_BSBY_R	9
SCART_RGB	10
AUD_SSB_R	11
AUD_SPI_MISO_R	12

[PAGE_TITLE=KSB, PCIEX + SMM GPIO + JTAG]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	24/74	24/74	C	1.0

KSB, SMC

N: DBG_LED0 PULLDOWN = SMC PRODUCTION MODE
DBG_LED0 PULLUP = SMC DEVELOPMENT MODE

U3D1 KSB IC

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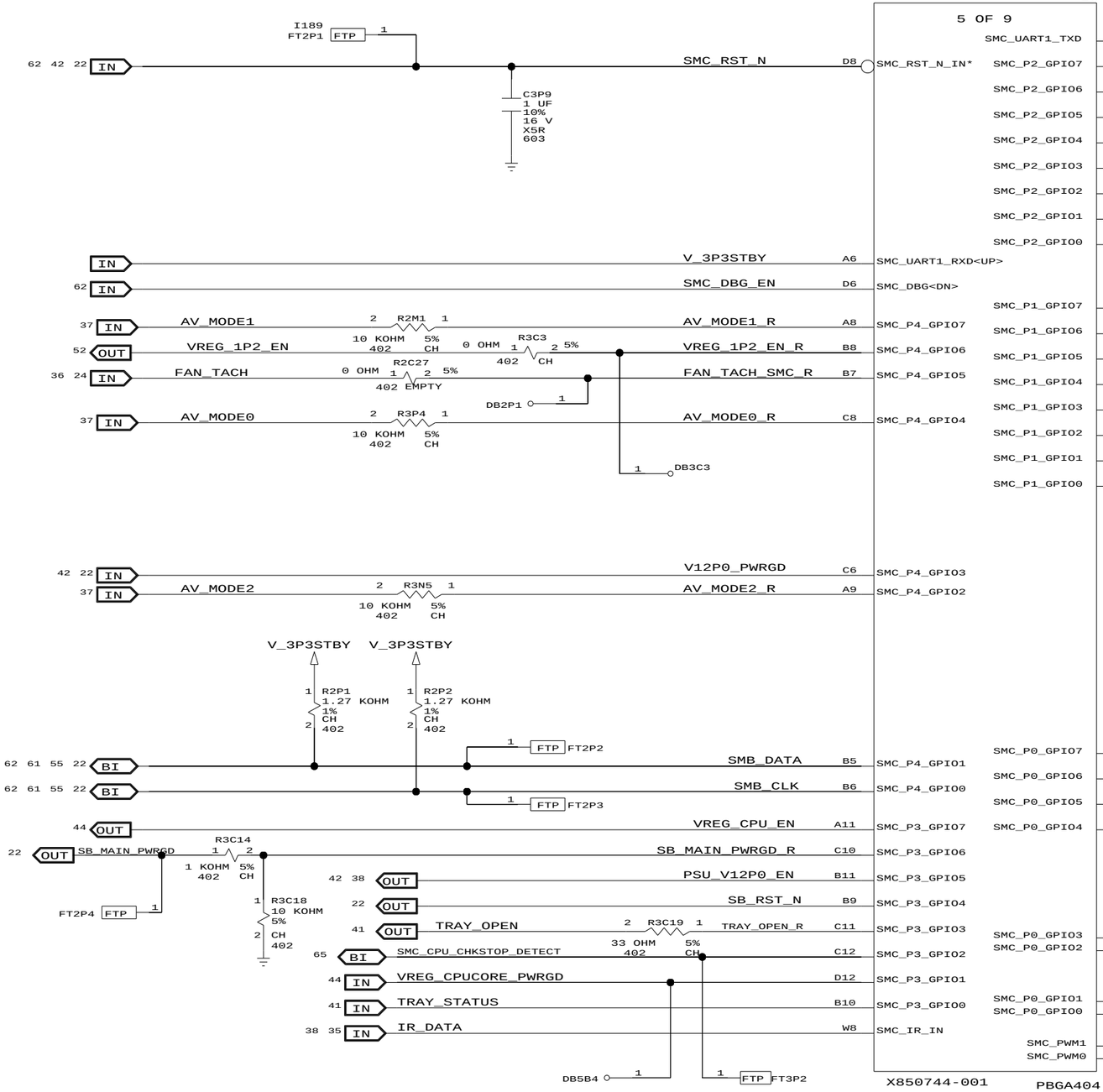


X850744-001 PBGA404

SMC_P2_GPIO7	W12	VREG_V5P0_EN	OUT	47	
SMC_P2_GPIO6	W13	DBG_LED0	OUT	65	
SMC_P2_GPIO5	Y11	EXT_TEMP_PWR_CTRL	OUT	61	DB3R5
SMC_P2_GPIO4	AB11	BINDSW_N	IN	38	
SMC_P2_GPIO3	AB10	VREG_VMEM_PWRGD	IN	50	
SMC_P2_GPIO2	AA11	VREG_VMEM_EN	OUT	50	
SMC_P2_GPIO1	AA12	VREG_VEDRAM_PWRGD	IN	49	
SMC_P2_GPIO0	Y12	VREG_V5P0_PWRGD	IN	47	DB2E2, DB2E3
SMC_P1_GPIO7	W11	VREG_V3P3_EN	OUT	48	DB2D1
SMC_P1_GPIO6	V9	TILTSW_N	IN	35	
SMC_P1_GPIO5	AA10	PWRSW_N	IN	35 38	
SMC_P1_GPIO4	Y10	VREG_VEDRAM_EN	OUT	49	
SMC_P1_GPIO3	Y9	EJECTSW_N	IN	35 38	
SMC_P1_GPIO2	W10	VREG_V5P0_SEL	OUT	46	
SMC_P1_GPIO1	AB9	VREG_V3P3_PWRGD	IN	48	
SMC_P1_GPIO0	W9	EXT_PWR_ON_N_R 2 R2C5 1 10 KOHM 5% 402 CH	EXT_PWR_ON_N IN	37 62 65 66	DB2C1, DB1E2
SMC_P0_GPIO7	Y13	GPU_RST_DONE_R	R3C16 47 OHM 5% 402 CH SMC_DBG_TXD OUT	62	
SMC_P0_GPIO6	AA14	CPU_RST_N	OUT	2	
SMC_P0_GPIO5	W14	SMC_P0_GPIO5	DB3R4		
SMC_P0_GPIO4	AB15	EXT_JTM_SEL	DB3R3		
SMC_P0_GPIO3	AB13	BORONFPM_DATA	BI	38	
SMC_P0_GPIO2	AB14	BORONFPM_CLK	BI	38	
SMC_P0_GPIO1	Y14	GPU_RST_N	OUT	4	
SMC_P0_GPIO0	AA13	CPU_PWRGD	OUT	2 65	
SMC_PWM1	D10	SMC_PWM1	OUT	36	
SMC_PWM0	D11	SMC_PWM0	OUT	23	DB3C1

V_3P3STBY
1 DEVKIT
R2G3 2 KOHM 1% CH 402 2
1 RETAIL DB2G3 1
R2G4 2 KOHM 1% CH 402 2

2 R3E6 1 GPU_RST_DONE IN 4
1 KOHM 5% 402 CH
1 R3E7 10 KOHM 5% 2 CH 402

V_1P8STBY
JTM_INT 1 R3R12 10 KOHM 5% 2 CH 402
JTM_EXT 1 R3R10 10 KOHM 5% 2 CH 402
1 R3R7 100 KOHM 5% 2 CH 402
1 R3R8 100 KOHM 5% 2 CH 402

PU: EXT JTM
PD: KSB JTM

DEBUG BUS

KSB PIN	DEBUG BUS BIT
SMC_P1_GPIO1	13
FAN_TACH	14
SMC_PWM0	15
SMC_P1_GPIO6	16
SMC_P2_GPIO0	17
SMC_P2_GPIO1	18
SMC_P2_GPIO3	19
SMC_P2_GPIO4	20
SMC_P2_GPIO5	21
SMC_P3_GPIO1	22
SMC_P3_GPIO2	23

SMC_P1,2,3,4 GPIOS ARE ON V3P3STBY. SMC_P0 GPIOS ARE ON 1P8VSTBY

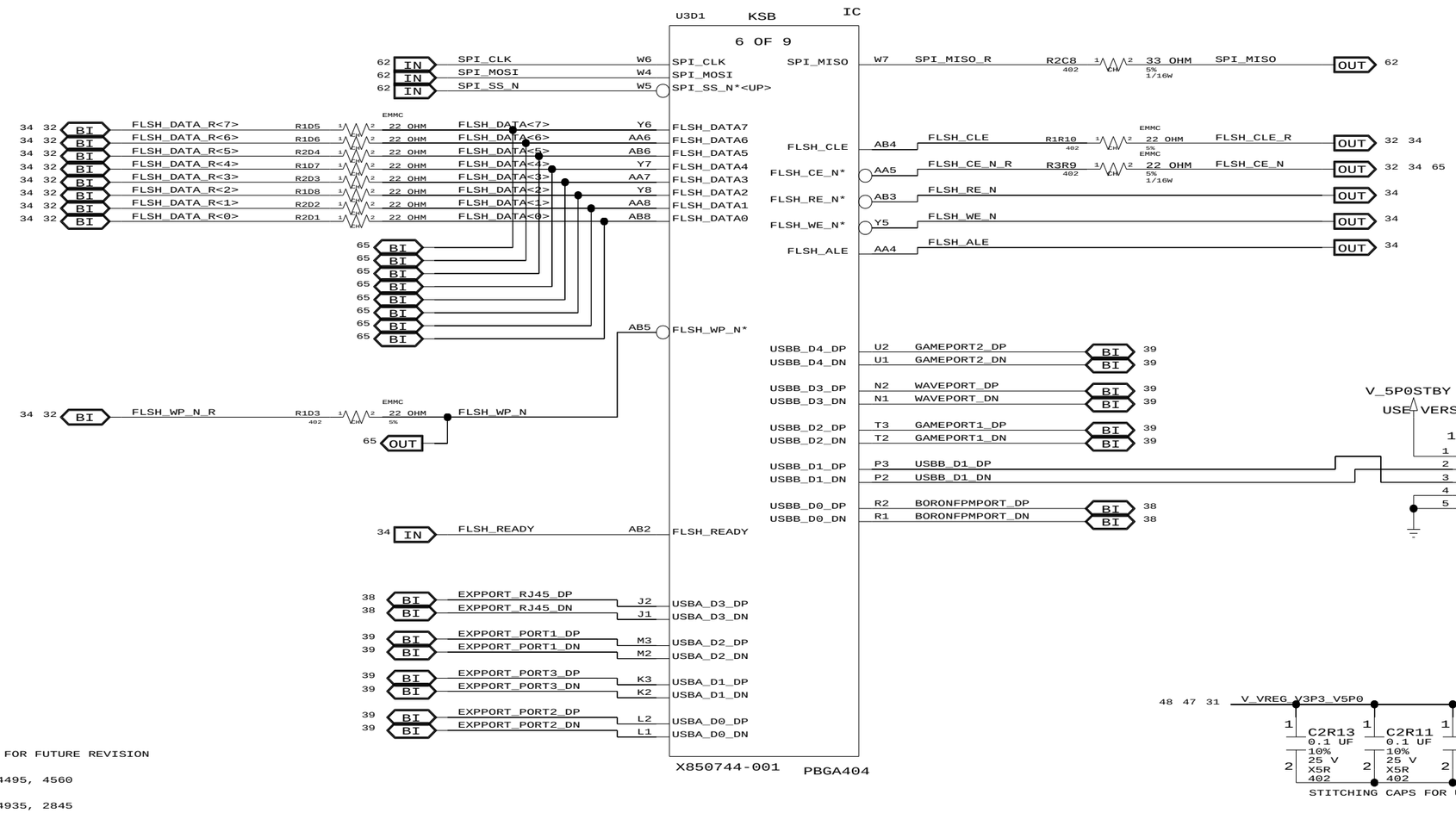
[PAGE_TITLE=KSB, SMC]

DRAWING
Fri Jan 04 12:07:17 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	25/74	25/74	C	1.0

KSB, FLASH + USB + SPI

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R1D5	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R1D6	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R2D4	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R1D7	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R2D3	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R1D8	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R2D2	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R2D1	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R1D3	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R1R10	X800967-001	CH	RES,0OHM,0402	NAND	PACK_IGNORE=TRUE
R3R9	X800451-001	CH	RES,10OHM,0402	NAND	PACK_IGNORE=TRUE

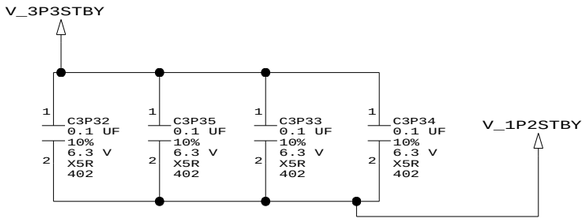


[PAGE_TITLE=KSB, FLASH + USB + SPI]

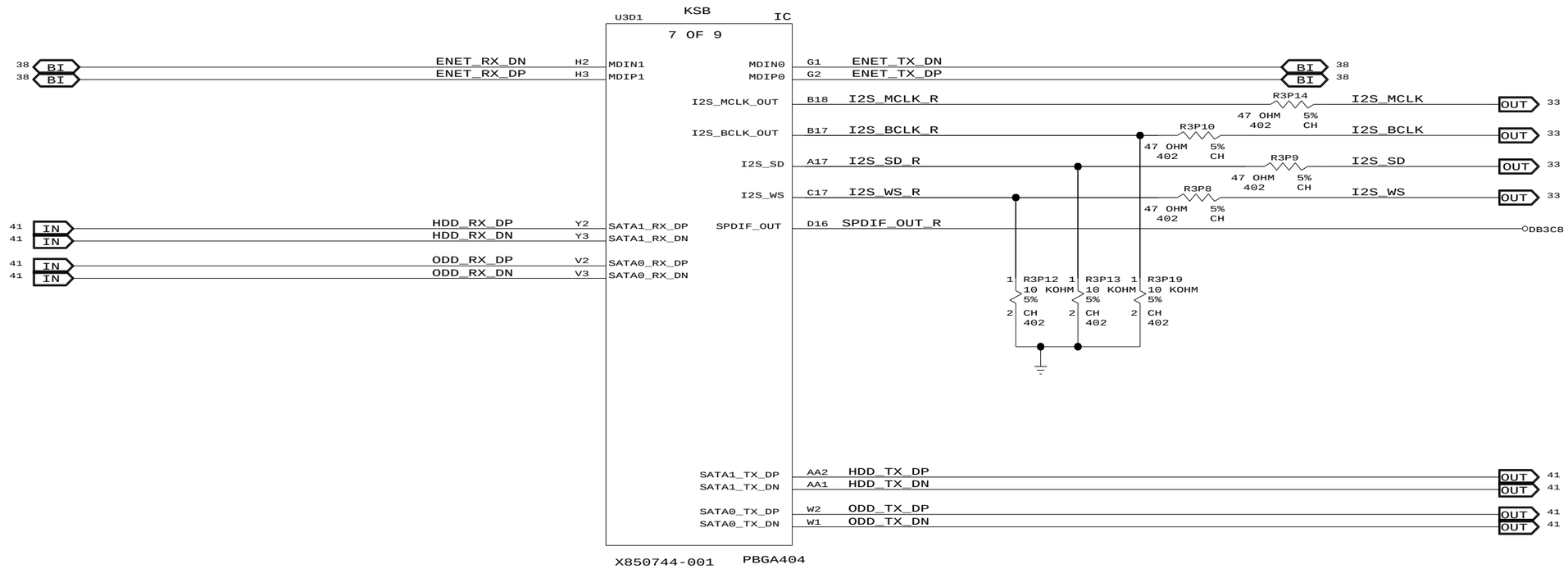
DRAWING
Fri Jan 04 12:07:17 2008

MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
CONFIDENTIAL	STINGRAY	26/74	26/74	C	1.0

KSB, ETHERNET + AUDIO + SATA



STITCHING CAPS FOR I2S SIGNALS,PARTICULARLY MCLK.
PLACE AS CLOSE AS POSSIBLE TO I2S_MCLK, I2S_BCLK, I2S_SD, AND I2S_WS.

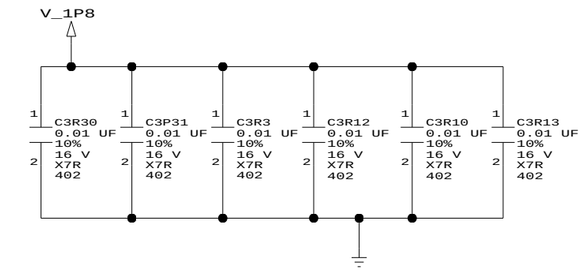


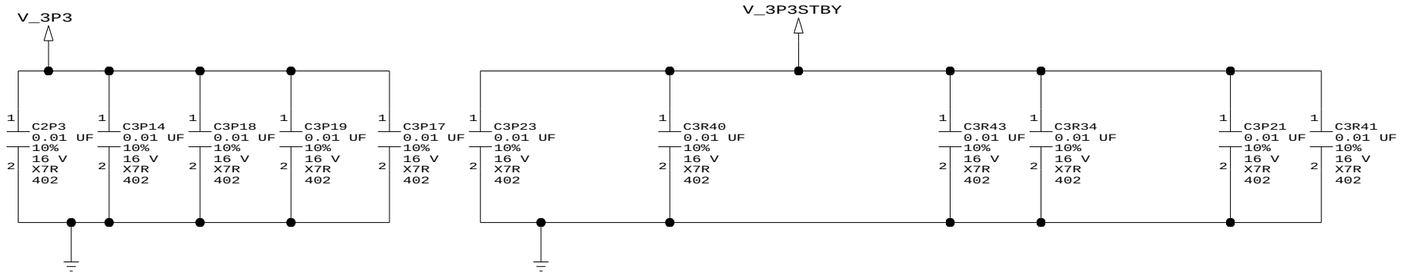
[PAGE_TITLE=KSB, ETHERNET + AUDIO + SATA]

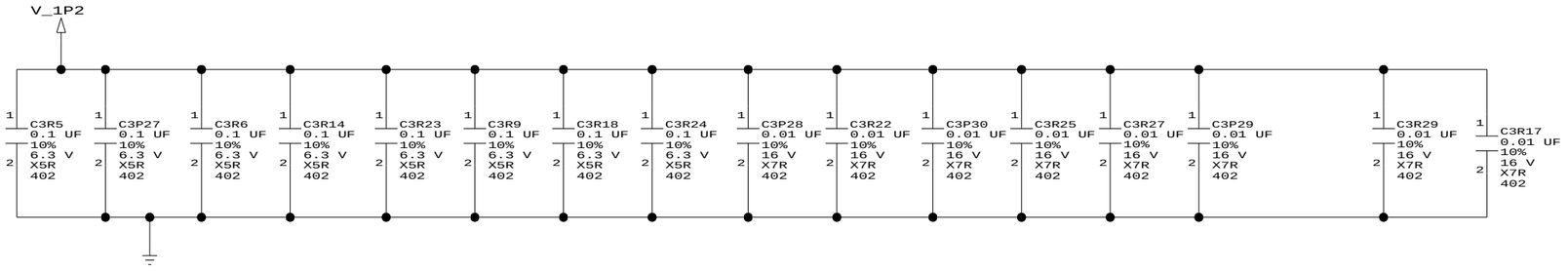
DRAWING
Fri Jan 04 12:07:18 2008

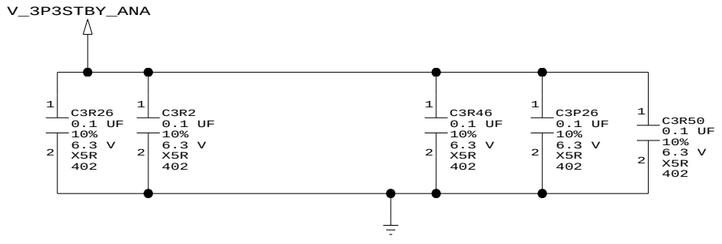
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	27/74	27/74	C	1.0

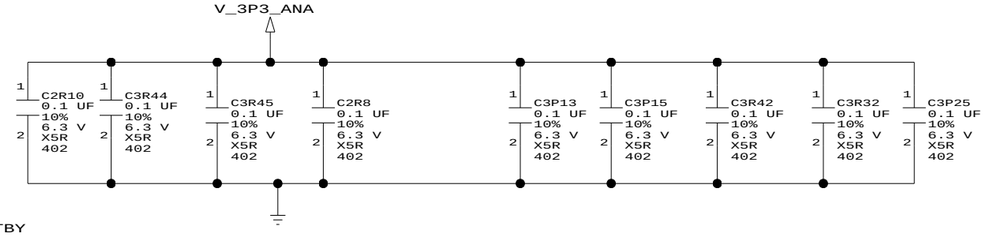
KSB,DECOUPLING

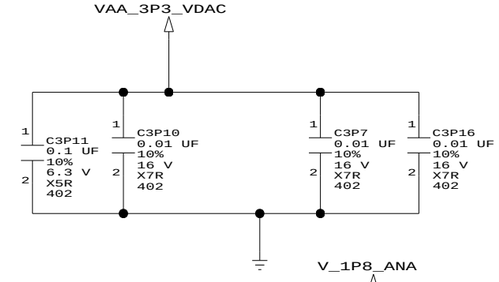


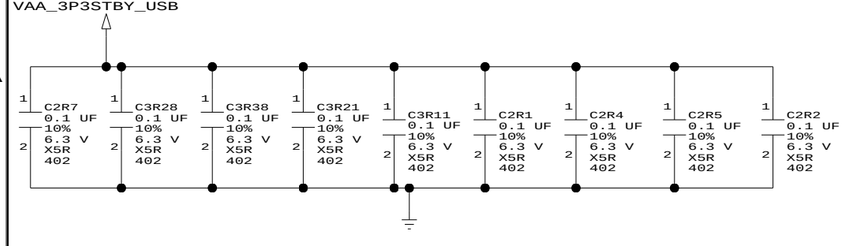


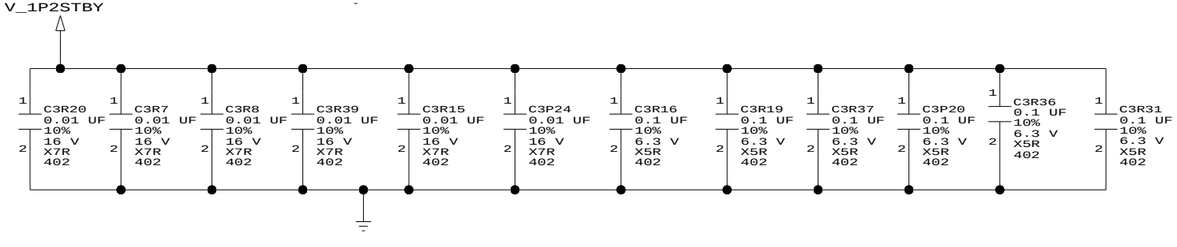


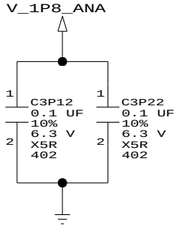












[PAGE_TITLE=KSB, DECOUPLING]

DRAWING
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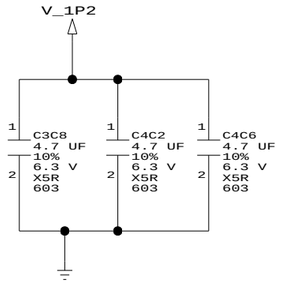
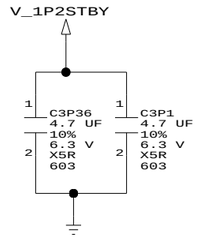
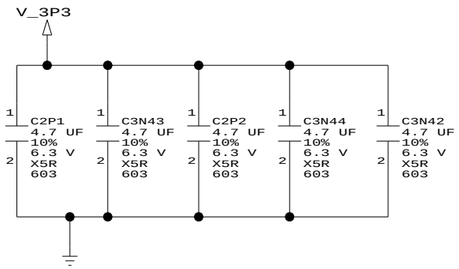
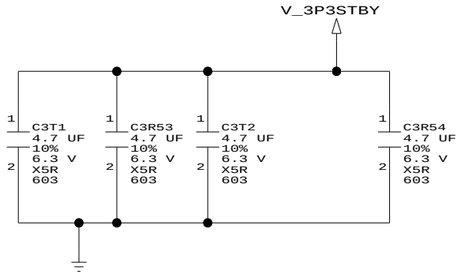
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	28/74	28/74	C	1.0

KSB, BULK DECOUPLING







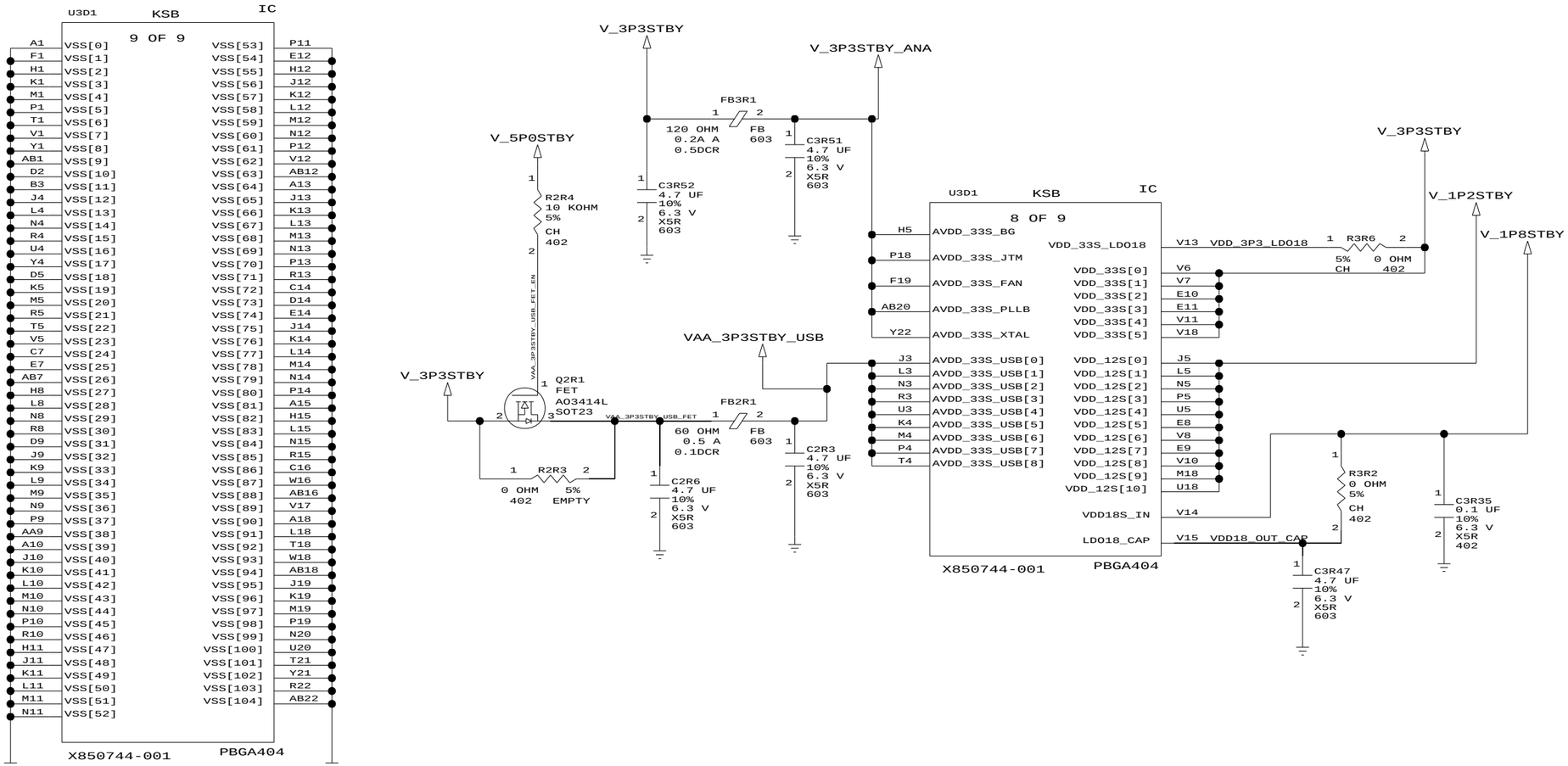


[PAGE_TITLE=KSB, BULK DECOUPLING]

DRAWING
Fri Jan 04 12:07:18 2008

PROJECT NAME	PAGE	CSA PAGE	FAB	REV
STINGRAY	29/74	29/74	C	1.0

KSB, STANDBY POWER + GROUND



[PAGE_TITLE=KSB, STANDBY POWER]

DRAWING
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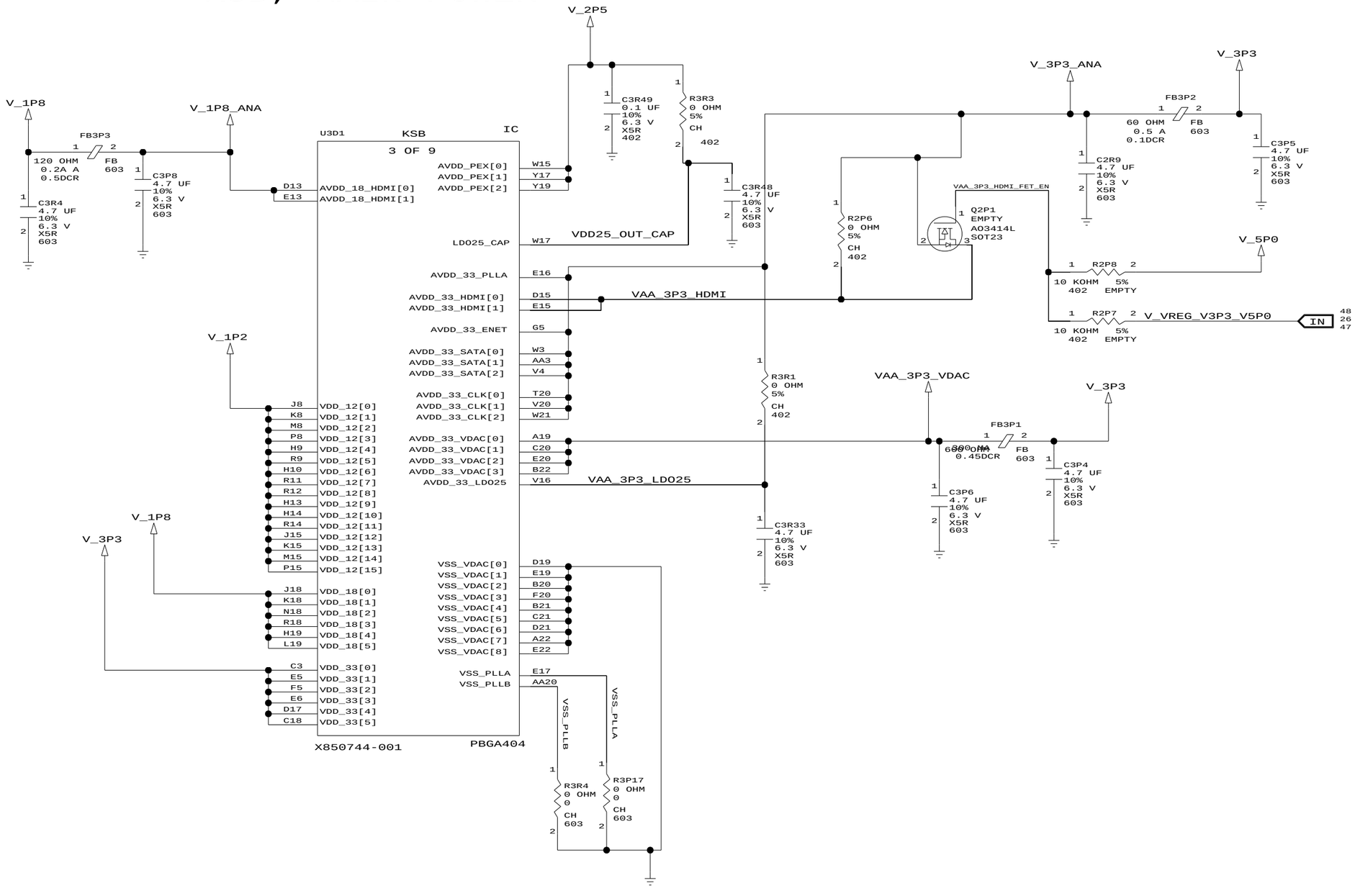
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	30/74	30/74	C	1.0

KSB, MAIN POWER



[PAGE_TITLE=KSB, MAIN POWER]

DRAWING
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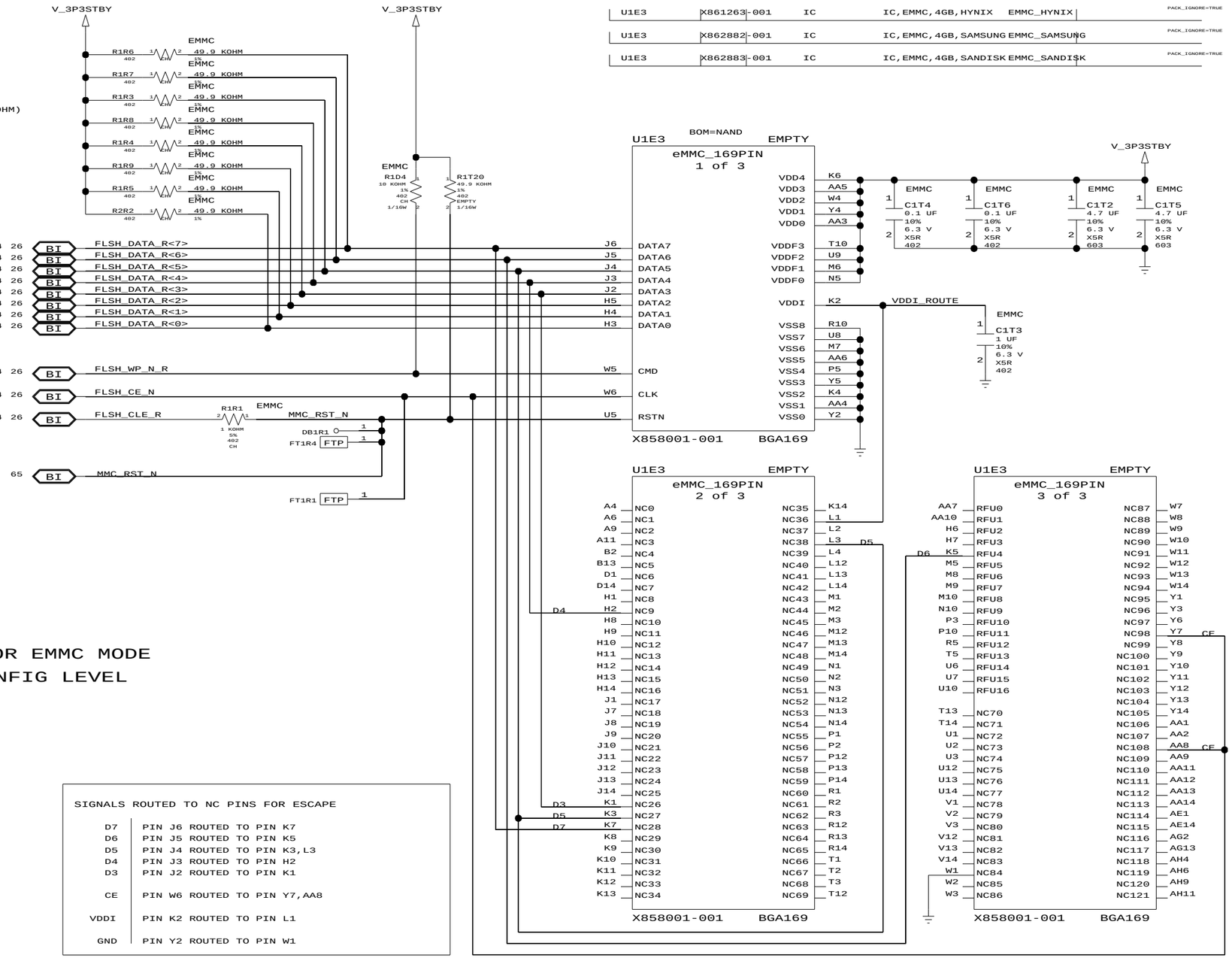
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	31/74	31/74	C	1.0

EMMC

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
U1E3	X861263-001	IC	IC,EMMC,4GB,HYNIX	EMMC_HYNIX PACK_IGNORE=TRUE
U1E3	X862882-001	IC	IC,EMMC,4GB,SAMSUNG	EMMC_SAMSUNG PACK_IGNORE=TRUE
U1E3	X862883-001	IC	IC,EMMC,4GB,SANDISK	EMMC_SANDISK PACK_IGNORE=TRUE

TOSHIBA 32NM NEEDED STRONGER PULLUPS (20KOHM)



ALL COMPONENTS ON THIS PAGE ARE FOR EMMC MODE
TO BE STUFFED/UNSTUFFED AT CONFIG LEVEL

SIGNALS ROUTED TO NC PINS FOR ESCAPE

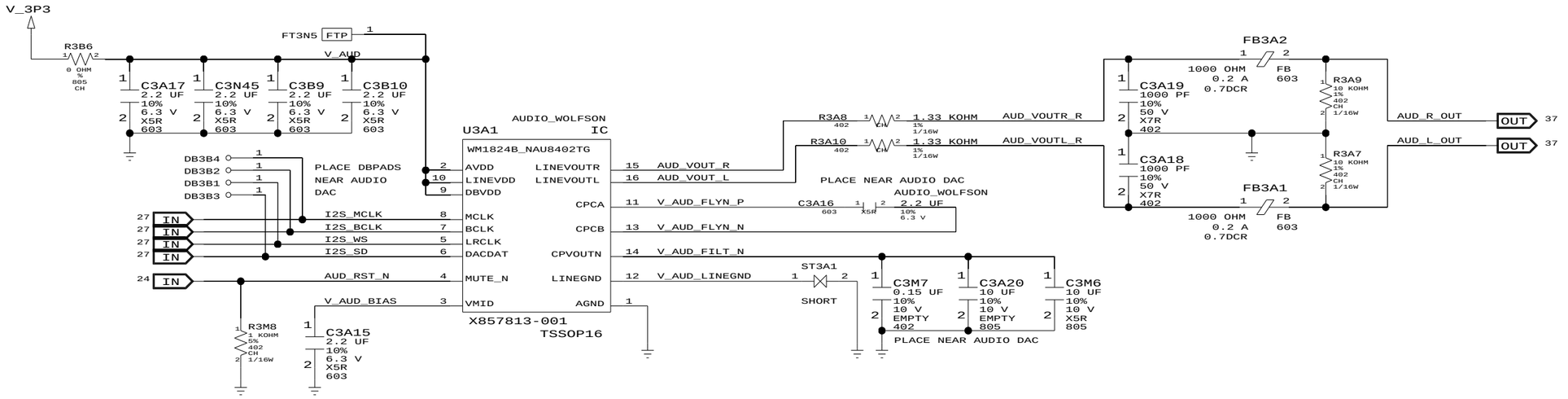
D7	PIN J6 ROUTED TO PIN K7
D6	PIN J5 ROUTED TO PIN K5
D5	PIN J4 ROUTED TO PIN K3,L3
D4	PIN J3 ROUTED TO PIN H2
D3	PIN J2 ROUTED TO PIN K1
CE	PIN W6 ROUTED TO PIN Y7,AA8
VDDI	PIN K2 ROUTED TO PIN L1
GND	PIN Y2 ROUTED TO PIN W1

[PAGE_TITLE=MMC + FLASH]

DRAWING
Fri Jan 04 12:07:19 2013

MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
CONFIDENTIAL	STINGRAY	32/74	32/74	C	1.0

KSB OUT, AUDIO



MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
U3A1	X858308-002	IC	IC,NAU8402WG AUDIO_NUVOTON	PACK_IGNORE=TRUE
C3A16	X800731-001	X7R	CAP,0.22UF,0603 AUDIO_NUVOTON	PACK_IGNORE=TRUE

[PAGE_TITLE=PSB OUT, AUDIO]

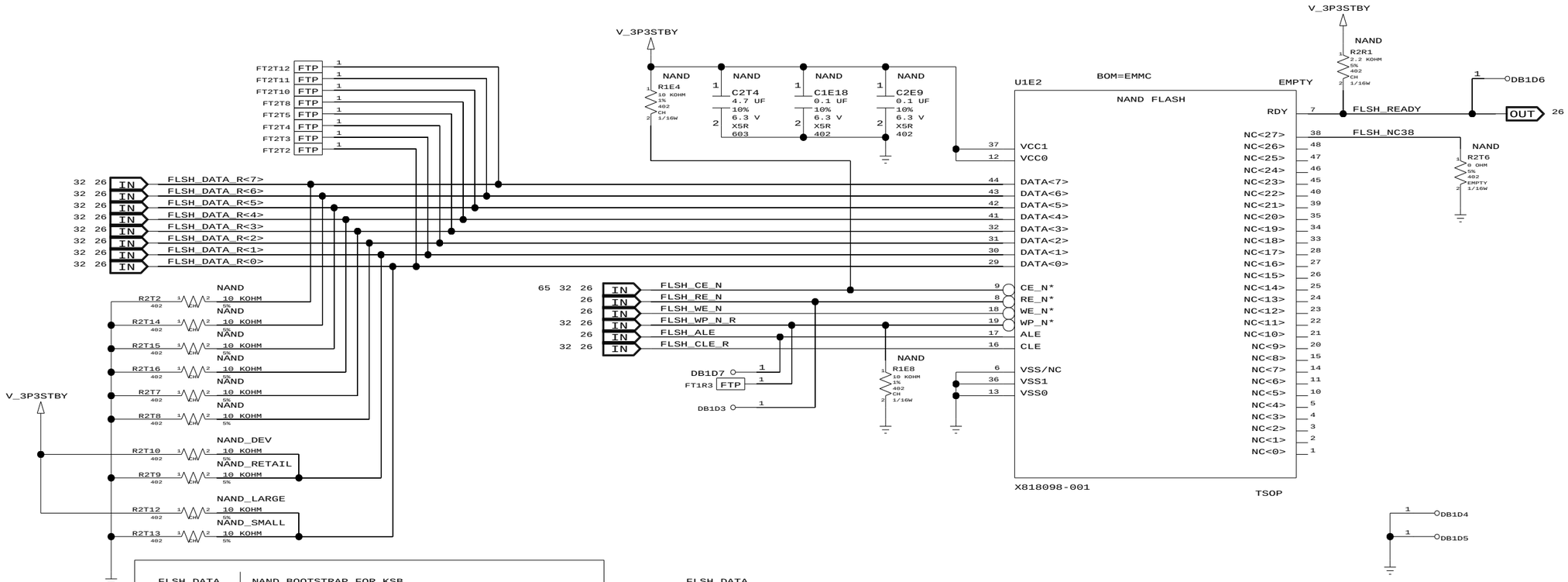
DRAWING
Fri Jan 04 12:07:19 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	33/74	33/74	C	1.0

KSB OUT, FLASH

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
U1E2	X803471-003	IC	IC,NAND,16MB	NAND_16MB_HYNIX	PACK_IGNORE=TRUE
U1E2	X818098-001	IC	IC,NAND,512MB	NAND_512MB_HYNIX	PACK_IGNORE=TRUE

ALL COMPONENTS ON THIS PAGE ARE FOR NAND MODE
TO BE STUFFED/UNSTUFFED AT CONFIG LEVEL



FLSH_DATA 1	FLSH_DATA 0	NAND BOOTSTRAP FOR KSB FLASH CONFIGURATION	CONFIG
LOW	LOW	0.5KB, 16KB BLOCKS, 128MBIT	RETAIL
LOW	HIGH	0.5KB, 16KB BLOCKS, 512MBIT	RETAIL
HIGH	LOW	2KB PAGES, 128KB BLOCKS, 1/2/4 GBIT	DEV
HIGH	HIGH	4KB PAGES, 256KB BLOCKS, 2/4/8 GBIT	DEV

FLSH_DATA
2 1 0

0 0 0 Raw NAND mode, 0.5kB, 16kB blocks, 128Mb
0 0 1 Raw NAND mode, 0.5kB, 16kB blocks, 512Mb
0 1 0 Raw NAND mode, 2.0kB, 128kB blocks, vary size
0 1 1 Raw NAND mode,
1 0 0 Raw NAND mode, 4.0kB, 256kB blocks, vary size
1 0 1 Raw NAND mode,
1 1 0 Raw NAND mode,
1 1 1 MMC mode

[PAGE_TITLE=PSB OUT, FLASH]

DRAWING
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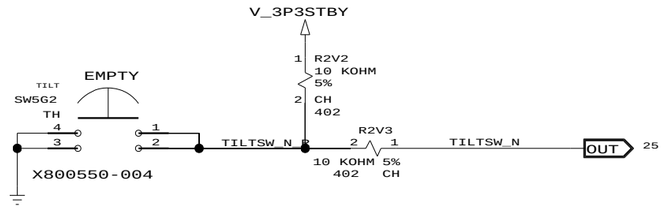
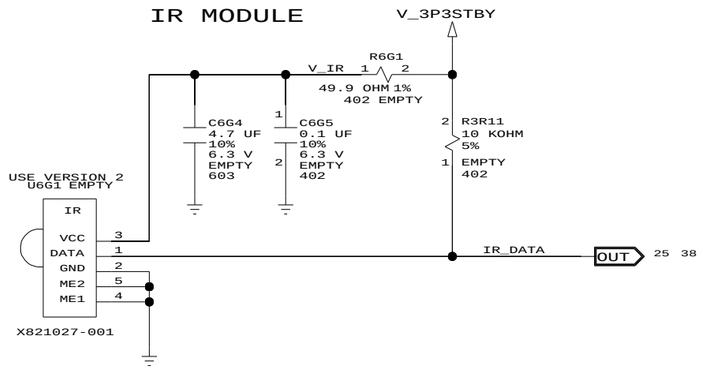
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	34/74	34/74	C	1.0

CONN, INFARED + SWITCHES + AUDIBLE F/B

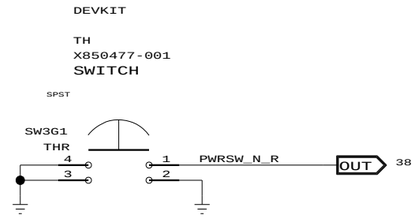
TILT SWITCH, SOLICO



IR MODULE

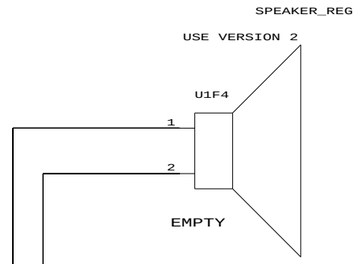


DEVKIT

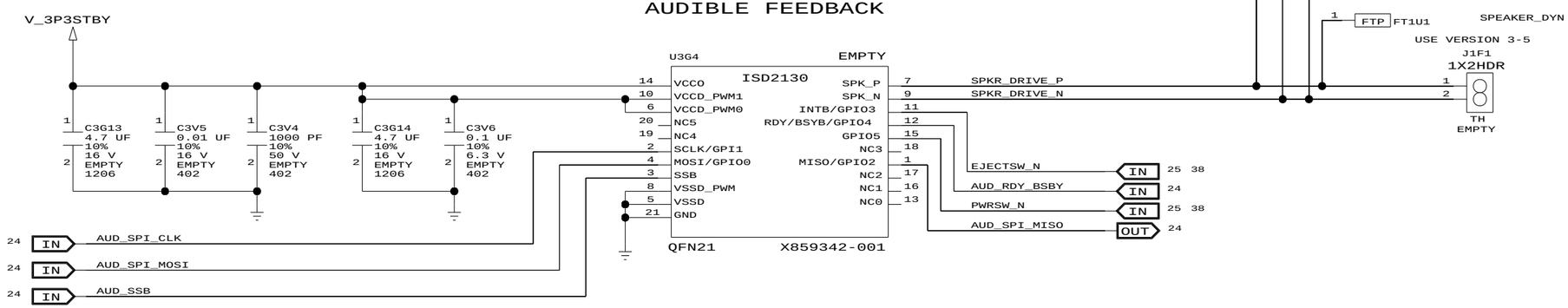


POWER BUTTON

SPEAKER_REG



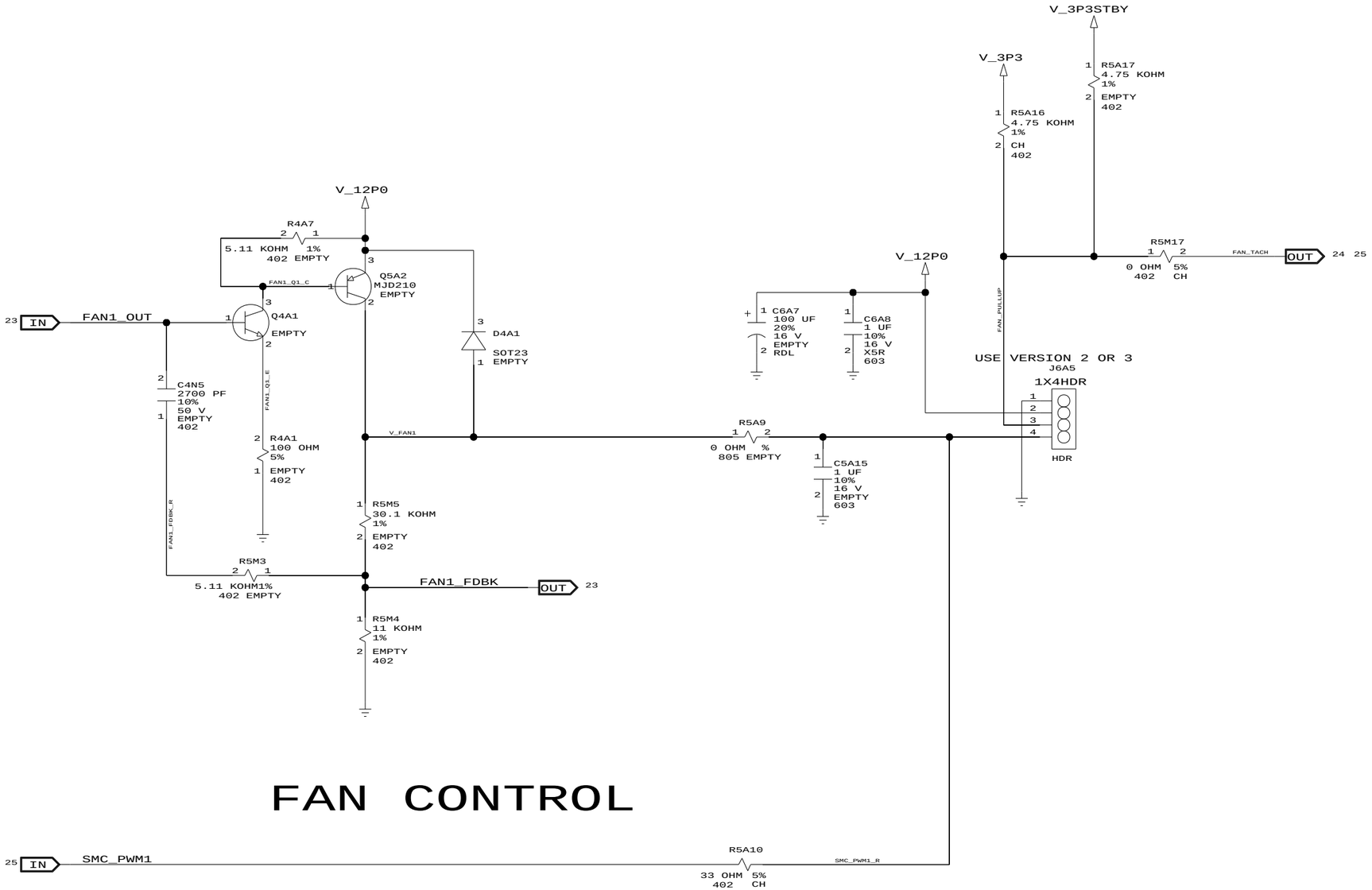
AUDIBLE FEEDBACK



[PAGE_TITLE=CONN,INFRARED+SWITCHES+AUDIBLE F/B]

DRAWING	MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
Fri Jan 04 12:07:19	2013 CONFIDENTIAL	STINGRAY	35/74	35/74	C	1.0

CONN, FAN



FAN CONTROL

[PAGE_TITLE= CONN, FAN]

DRAWING
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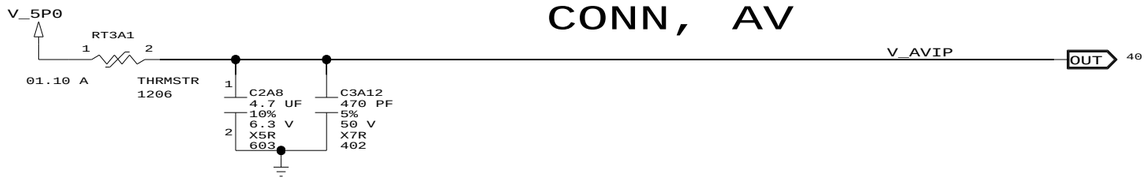
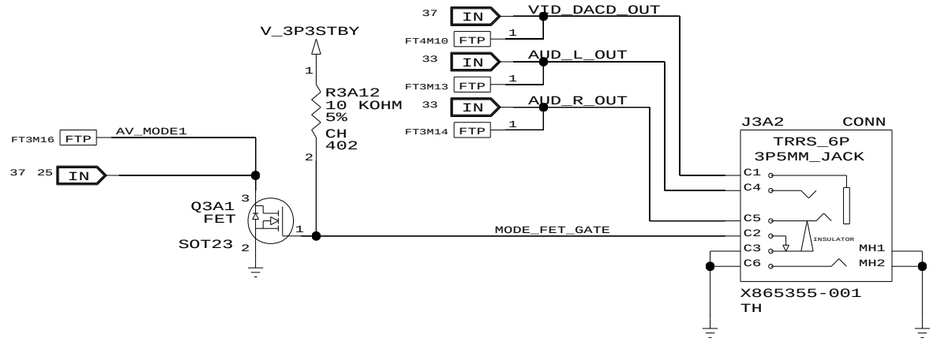
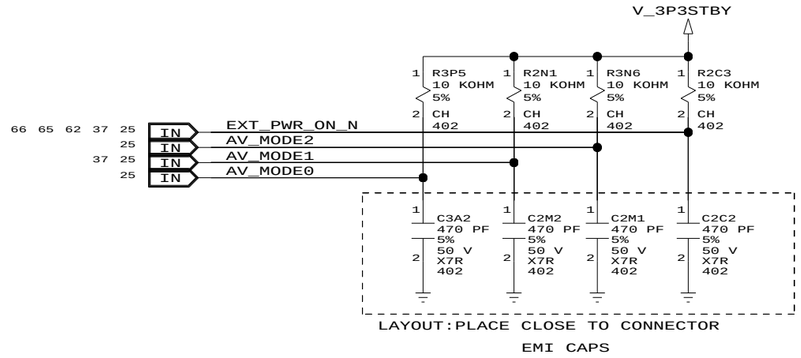
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 36/74	CSA PAGE 36/74	FAB C	REV 1.0

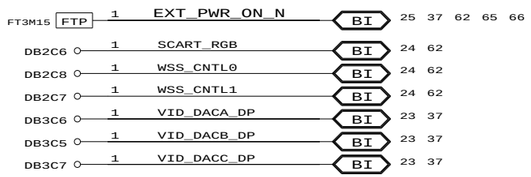
CONN, AV

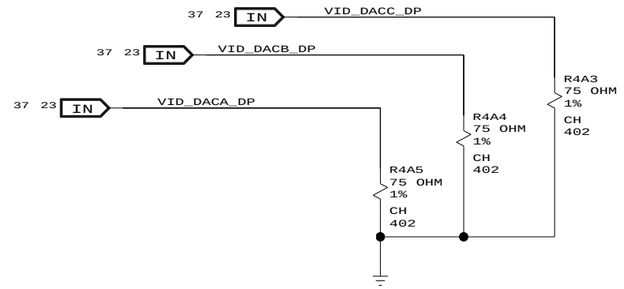
DAC	STANDARD	ADVANCED	SDTV	HDTV	SCART	VGA
A	N/A	Y(LUMA)	Y	Y	G	G
B	N/A	C(CHROMA)	PR	PR	R	R
C	N/A	N/A	PB	PB	B	B
D	CVBS(COMP)	CVBS(COMP)	CVBS	N/A	CVBS	CVBS

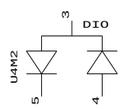


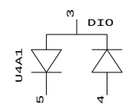


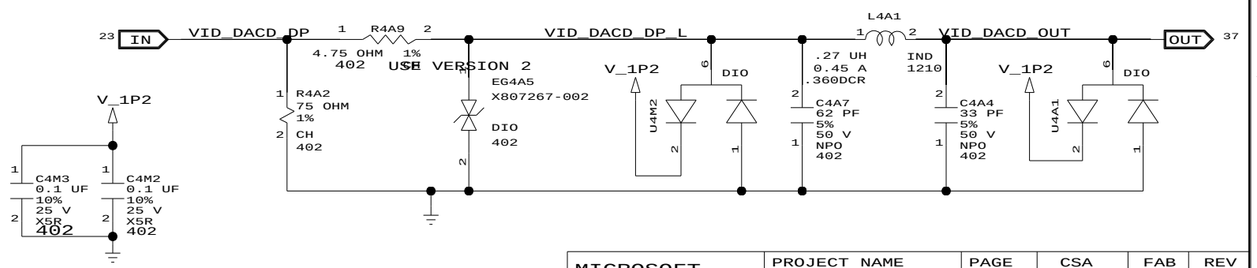












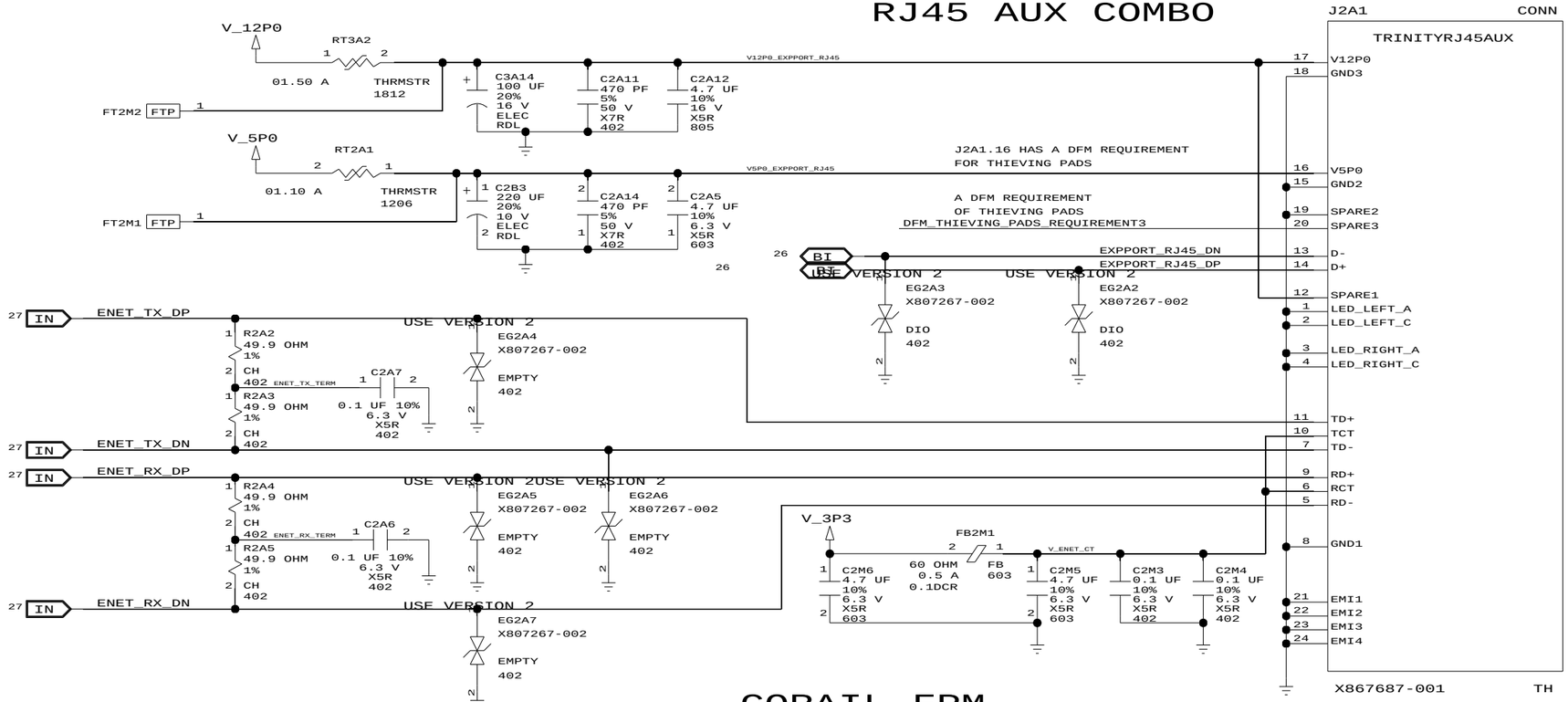
DRAWING
Fri Jan 04 12:07:20 2008

MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
CONFIDENTIAL	STINGRAY	37/74	37/74	C	1.0

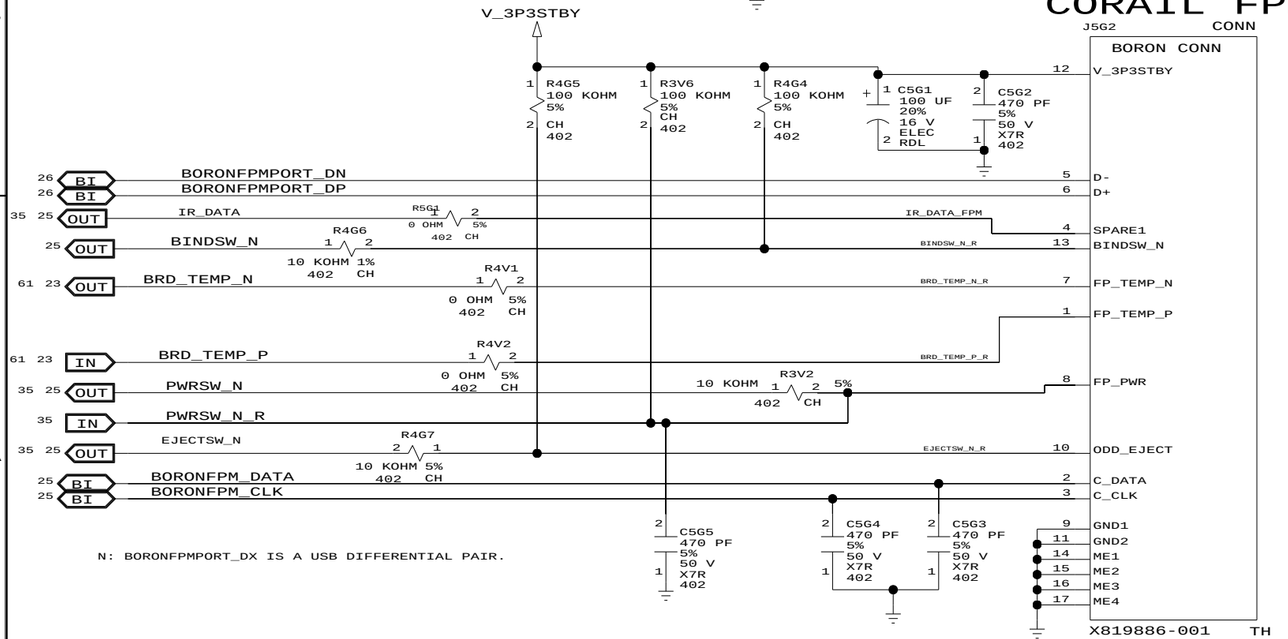
[PAGE_TITLE=[CONN, AVIP]

CONN, RJ45 USB AUX COMBO + CORAIL + PWR

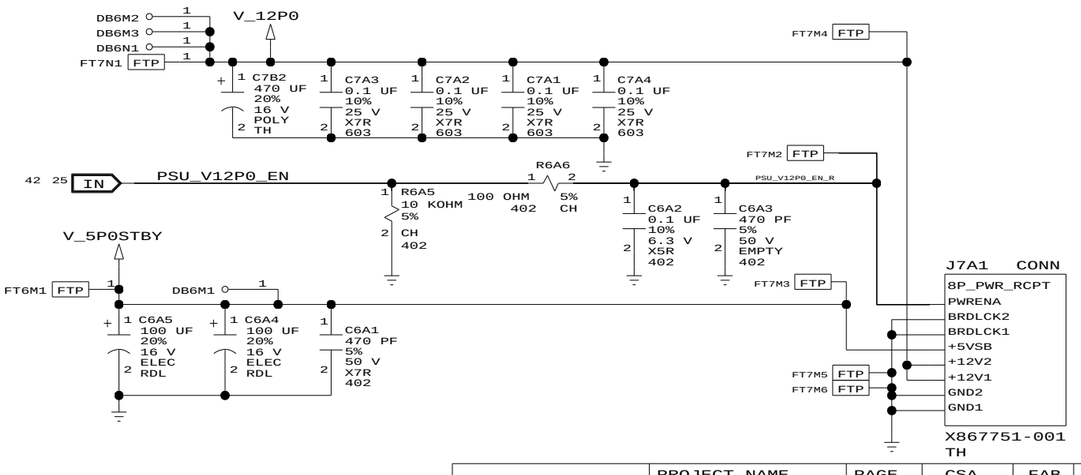
RJ45 AUX COMBO



CORAIL FPM



POWER



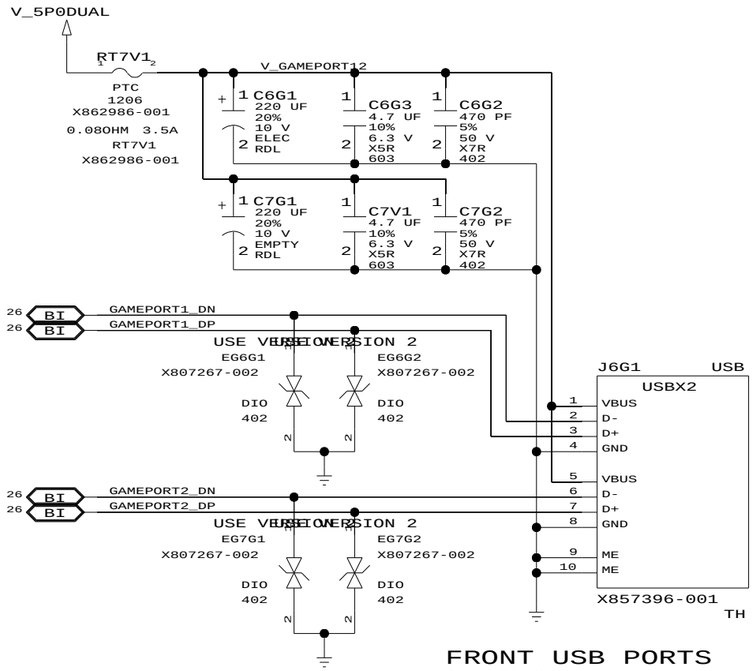
[PAGE_TITLE=CONN, RJ45 AUX COMBO + CORAIL + PWR]

DRAWING
Fri Jan 04 12:07:20 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	38/74	38/74	C	1.0

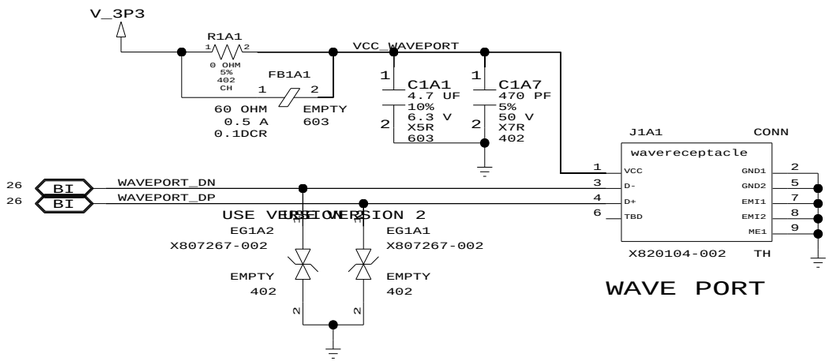
CONN, USB + MEM PORTS + WAVEPORT

N: ALL DIFFERENTIAL PAIRS ON THIS PAGE ARE USB DIFFERENTIAL PAIRS.

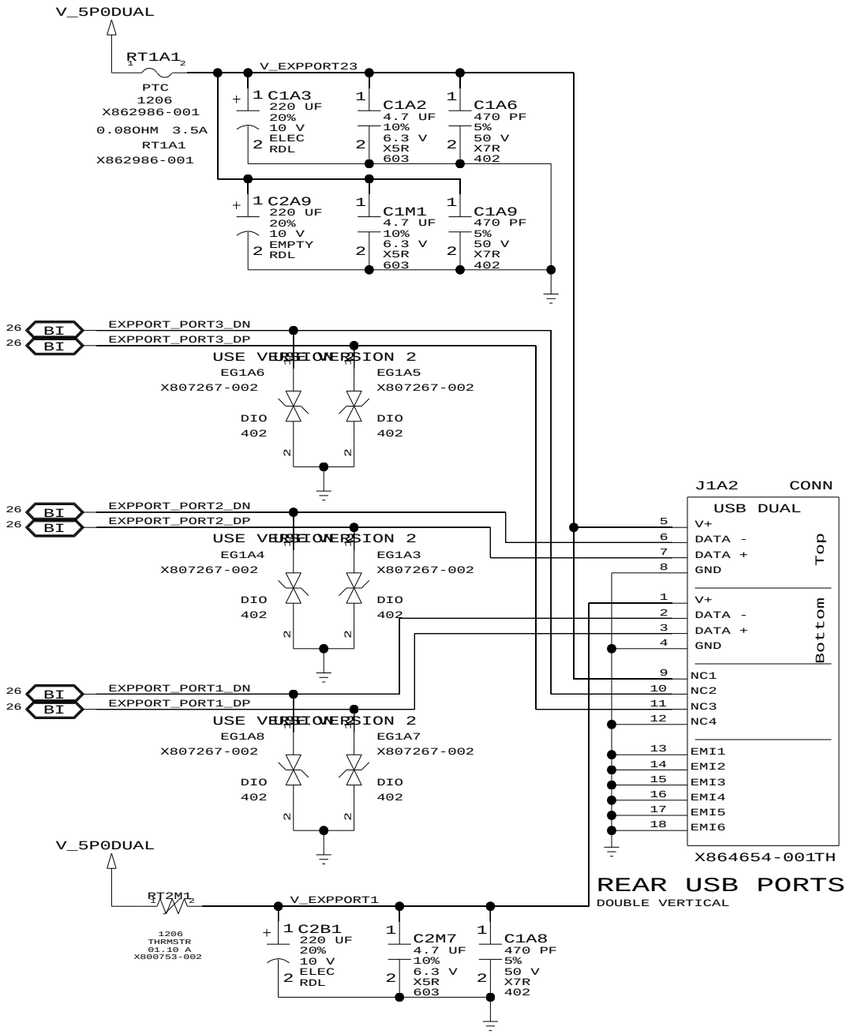


FRONT USB PORTS

DUAL HORIZONTAL



WAVE PORT



REAR USB PORTS

DOUBLE VERTICAL

[PAGE_TITLE=CONN, MEMORY PORTS + GAME PORTS]

DRAWING
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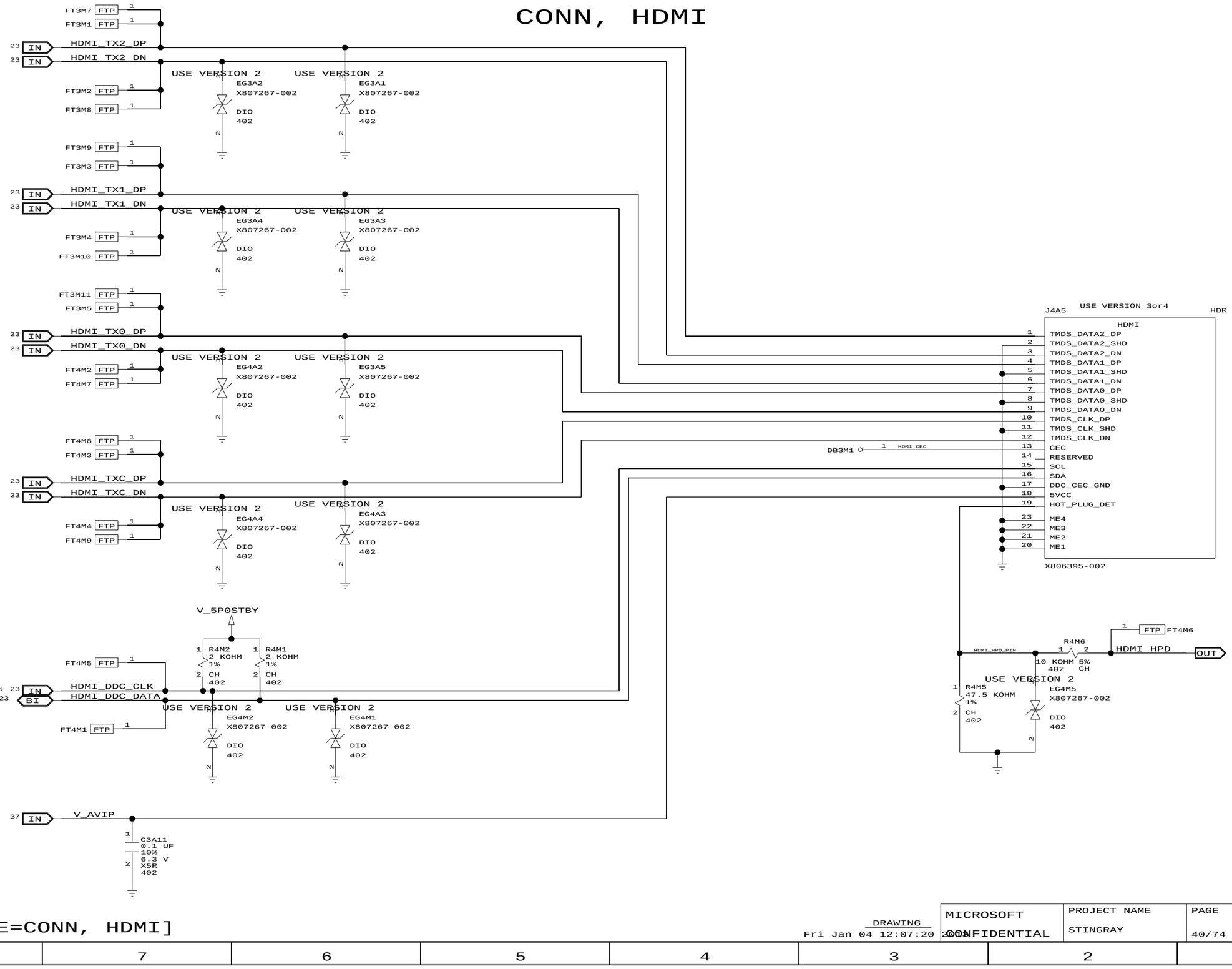
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 39/74	CSA PAGE 39/74	FAB C	REV 1.0

CONN, HDMI



[PAGE_TITLE=CONN, HDMI]

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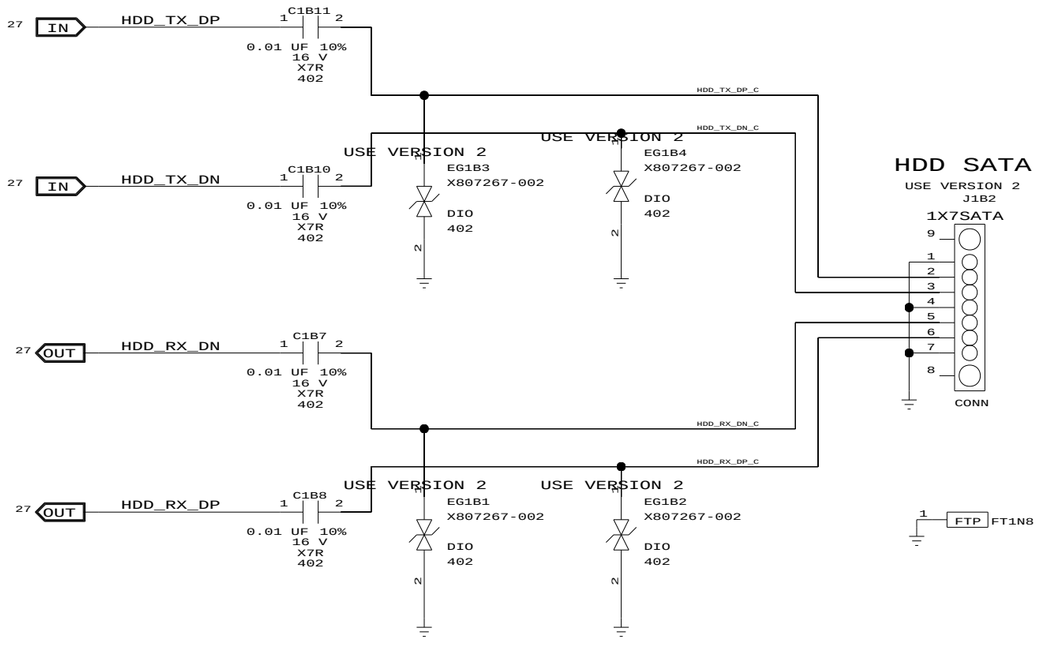
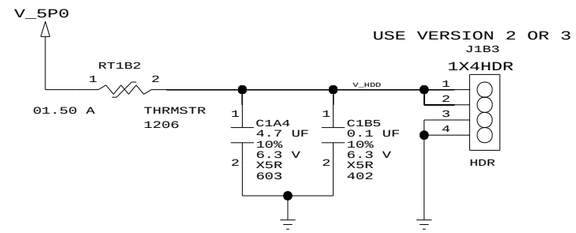
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	40/74	40/74	C	1.0

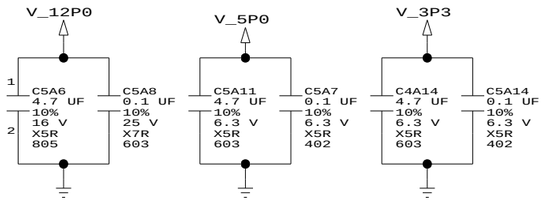
CONN, ODD + HDD



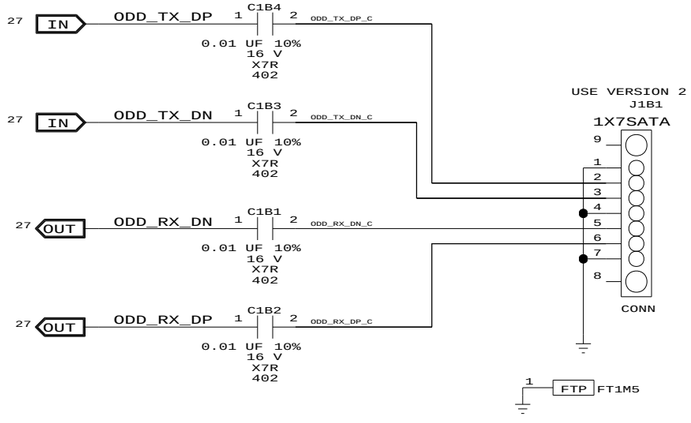
HDD POWER



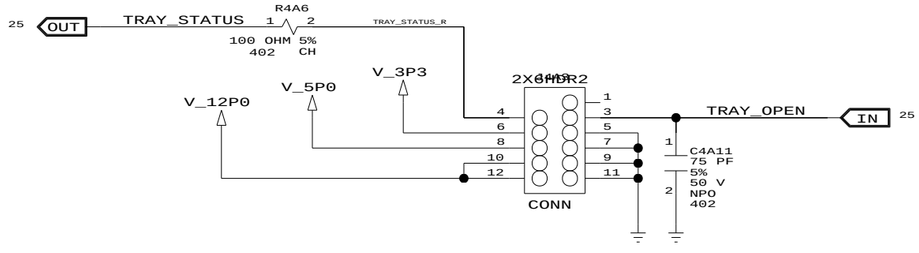
ODD POWER DECOUPLING



ODD SATA



ODD POWER AND CONTROL



[PAGE_TITLE=CONN, ODD + HDD + MU]

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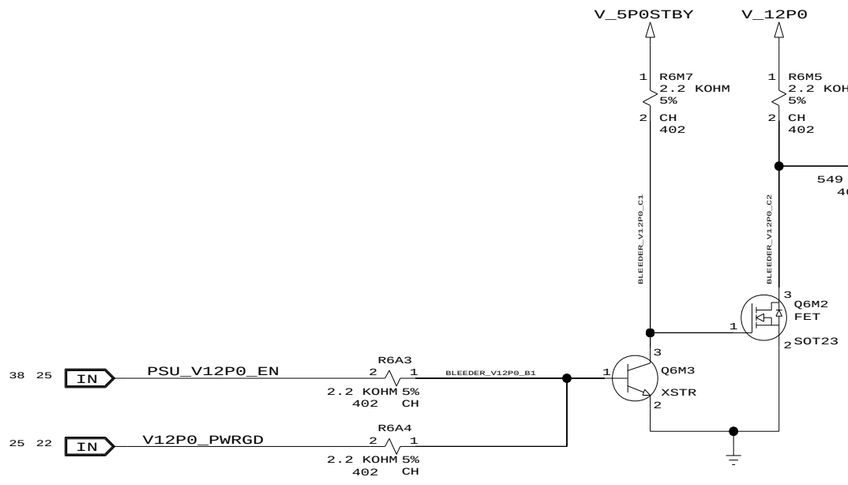
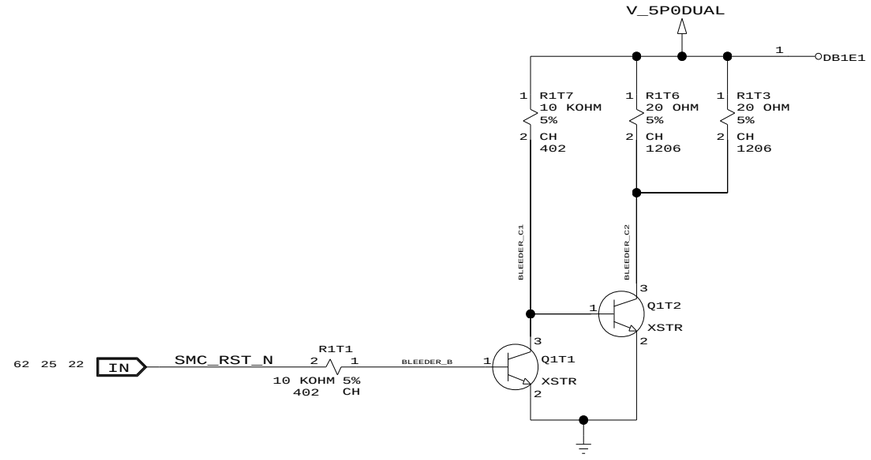
Fri Jan 04 12:07:21 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	41/74	41/74	C	1.0

VREG, BLEEDERS



V_12P0 & V_5P0 BLEEDERS



V_5P0DUAL BLEEDER

[PAGE_TITLE= VREGS,_BLEEDERS]

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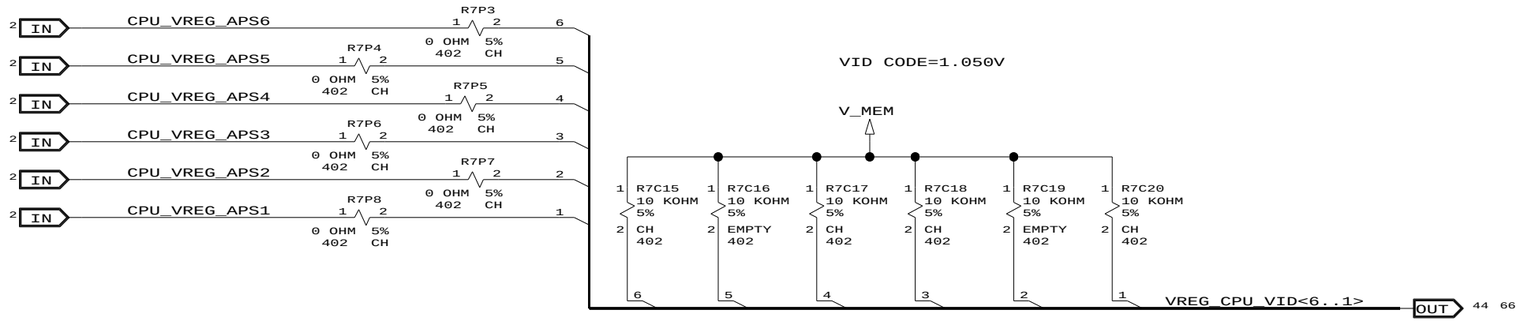
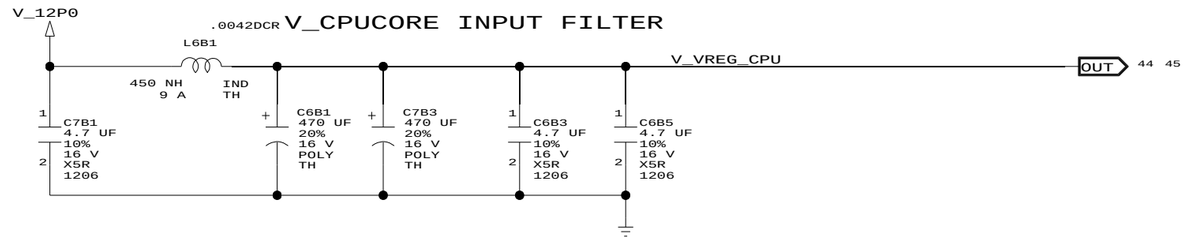
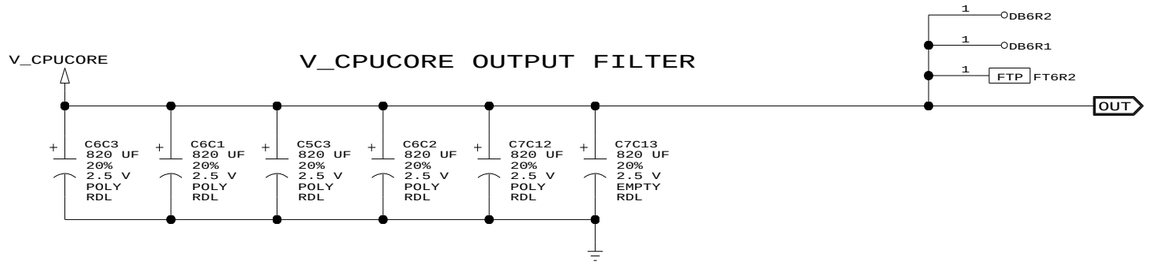
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 42/74	CSA PAGE 42/74	FAB C	REV 1.0

VREGS, INPUT + OUTPUT FILTERS







[PAGE_TITLE=VREGS, INPUT + OUTPUT FILTERS]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	43/74	43/74	C	1.0

VREGS, CPU CONTROLLER

45 43 IN V_VREG_CPU
R7C26 603 1 CH 2 681 OHM 1% 1/16W
VREG_CPU_VCC
R7C25 603 1 CH 2 681 OHM 1% 1/16W
R7B5 402 1 CH 2 1 KOHM 5% 1/16W
VREG_CPU_RAMPADJ_R
R7C22 1 422 KOHM 1% 402 CH 2
RRAMP
C7C2 1 0.1 UF 10% 25 V X7R 603 2
FT3P8 FTP 1
C7C23 1 4.7 UF 10% 16 V X5R 1206 2
C7C22 1 1 UF 10% 16 V X5R 603 2
VREG_CPU_VCC3_3P3
C7C20 1 0.1 UF 10% 6.3 V X5R 402 2
25 IN VREG_CPU_EN
R7C31 1 10 KOHM 5% 402 CH 1/16W 2
66 60 59 58 57 56 55 IN PMBUS_CLK
66 60 59 58 57 56 55 BI PMBUS_DATA
45 IN VREG_CPU_PHASE2
R7C23 402 1 CH 2 0 OHM 5% 1/16W
45 IN VREG_CPU_PHASE1
R7C24 402 1 CH 2 0 OHM 5% 1/16W
66 OUT VREG_CPU_CSCOMP
R7B1 35.7 KOHM 1% 402 CH 1/16W
RT6C1 603 THRMSTR XB01015-001
RCS1
RTH1 TEMP SENSOR
R7C21 6.81 KOHM 1% 402 CH 1/16W
VREG_CPU_CSCOMP_R
R7B3 27.4 KOHM 1% 402 CH 1/16W
R7B4 27.4 KOHM 1% 402 CH 1/16W
R7B2 52.3 KOHM 1% 402 CH 1/16W
RPH2
RPH1
RCS2
C7C15 3300 PF 10% 50 V X7R 402
C7C14 3300 PF 10% 50 V X7R 402
CCS2
CCS1
66 OUT VREG_CPU_CSSUM
66 OUT VREG_CPU_CSREF
V_CPUCORE
C7P1 1000 PF 10% 50 V X7R 402
ST6B3 SHORT OFFGRID
PLACE SHORT NEXT TO OUTPUT OF DUAL INDUCTOR
ST6D1 SHORT OFFGRID
PLACE SHORT NEXT TO POINT OF LOAD
DB7C1
VREG_V_CPUCORE_S
VENABLE
R7C32 0 OHM % 805 EMPTY
C7C16 470 PF 5% 402 X7R 50 V CB
C7C17 10 PF 5% 402 NPO 50 V CFB
R7P9 1.1 KOHM 1% 402 CH RB
C7C18 1500 PF 10% 402 X7R 50 V CA
R7P10 18.2 KOHM 1% 402 CH RA
DB7C2
ST6D2 SHORT OFFGRID
PLACE SHORT NEXT TO POINT OF LOAD

U7C1 IC NCP4202

1	VCC3				
21	VCC				
VREG_CPU_VCC					
VREG_CPU_RAMPADJ	8	RAMPADJ	PWRGD	28	VREG_CPUCORE_PWRGD OUT 25
VREG_CPU_EN	4	EN	IPD VID6	22	VREG_CPU_VID<6> IN 43 66
			IPD VID5	23	VREG_CPU_VID<5> IN 43 66
			IPD VID4	24	VREG_CPU_VID<4> IN 43 66
			IPD VID3	25	VREG_CPU_VID<3> IN 43 66
			IPD VID2	26	VREG_CPU_VID<2> IN 43 66
			IPD VID1	27	VREG_CPU_VID<1> IN 43 66
PMBUS_CLK	3	SCL			
PMBUS_DATA	2	SDA			
VREG_CPU_PHASE2_R	17	SW2			
VREG_CPU_PHASE1_R	18	SW1			
VREG_CPU_CSCOMP	14	CSCOMP	PWM2	19	VREG_CPU_PWM2 OUT 45
			PWM1	20	VREG_CPU_PWM1 OUT 45
VREG_CPU_CSSUM	13	CSSUM	OD1_N	16	VREG_CPU_DRV_EN OUT 45
VREG_CPU_CSREF	12	CSREF	IMON	5	VREG_CPU_IMON
VREG_CPU_FB	11	FB	RT	7	VREG_CPU_RT
VREG_CPU_COMP	10	COMP			
VREG_CPU_FBRTN	9	FBRTN			
VREG_CPU_IREF	6	IREF			
VREG_CPU_ILIMITFS	15	ILIMITFS	MPAD	29	

X857741-001 QFN29

R7C27 10 KOHM 5% 402 CH 1/16W 2
R7C28 909 KOHM 1% 402 CH 1/16W 2 X812615-001
ROSC=909K
FOSC=250KHZ
R7C29 121 KOHM 1% 402 CH 1/16W 2
NEED TO SET DURING VALIDATION

PARTS ARE TRIMMED AT FACTORY SUCH THAT VBOOT=1.05V

I2C ADDRESS
1100 000 R/W HEX
WRITE 1100 000 0 0XC0
READ 1100 000 1 0XC1

C7C21 0.1 UF 10% 402 X5R 6.3 V
R7C30 5.76 KOHM 1% 402 CH 1/16W
NOTE: VALID UP TO 58A
C7C19 1000 PF 10% 50 V X7R 402

[PAGE_TITLE=VREGS, CPU CONTROLLER]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	44/74	44/74	C	1.0

VREG, CPU OUTPUT PHASE 1 & 2

44 43 IN V_VREG_CPU

R6N1 2.2 OHM 1% 805 CH — VREG_CPU2_VCC — C6B4 1 UF 10% 16 V X5R 603

D6B1 SOT23 DIO

VREG_CPU_BST2 — C6N1 0.01 UF 10% 50 V EMPTY 805

R6N2 2.2 OHM 1% 805 CH — VREG_CPU_BST2_R — C6N2 0.1 UF 10% 25 V X7R 603

U6B1 IC — MOS DRIVER — X850497-001

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

44 IN VREG_CPU_PWM2

44 IN VREG_CPU_DRV_EN

VREG_CPU_DRVH2

VREG_CPU_DRVL2

Q6B2 X857866-001 DPAK_G1D2S3 FET

Q6C2 X857867-001 DPAK_G1D2S3 FET

Q6C1 X857867-001 DPAK_G1D2S3 FET

C7B5 4.7 UF 10% 16 V X5R 1206

C7N1 4.7 UF 10% 16 V EMPTY 1206

R6C1 1 OHM 1% CH 805 — VREG_CPU_SW2_R — C7C8 2200 PF 10% 50 V X7R 805

V_CPUCORE
NOM.VOLTAGE: 0.9-1.2V

VREG_CPU_PHASE2 OUT 44

V_CPUCORE

L6C1 SM EMPTY
DUAL INDUCTOR
L1 L4 L3 L2
X820048-001
420NH

DB7C4

DCR +/-8%

V_CPUCORE

L6C2 IND
DUAL INDUCTOR
L2 L3 L4 L1
X850592-001
420NH
40 A

+/-4%

NOTE: THRUHOLE PART IS 2% IMPROVEMENT ON DCR

R5N7 2.2 OHM 1% 805 CH — VREG_CPU1_VCC — C5B10 1 UF 10% 16 V X5R 603

D5B1 SOT23 DIO

VREG_CPU_BST1 — C5N5 0.01 UF 10% 50 V EMPTY 805

R5N8 2.2 OHM 1% 805 CH — VREG_CPU_BST1_R — C5N6 0.1 UF 10% 25 V X7R 603

U5B5 IC — MOS DRIVER — X850497-001

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

44 IN VREG_CPU_PWM1

VREG_CPU_DRVH1

VREG_CPU_DRVL1

Q6B1 X857866-001 DPAK_G1D2S3 FET

Q5C3 X857867-001 DPAK_G1D2S3 FET

Q5C1 X857867-001 DPAK_G1D2S3 FET

C6B2 4.7 UF 10% 16 V X5R 1206

C6N3 4.7 UF 10% 16 V EMPTY 1206

R5C1 1 OHM 1% CH 805 — VREG_CPU_SW1_R — C5C1 2200 PF 10% 50 V X7R 805

VREG_CPU_PHASE1 OUT 44

[PAGE_TITLE=VREGS, CPU OUTPUT PHASE 1,2]

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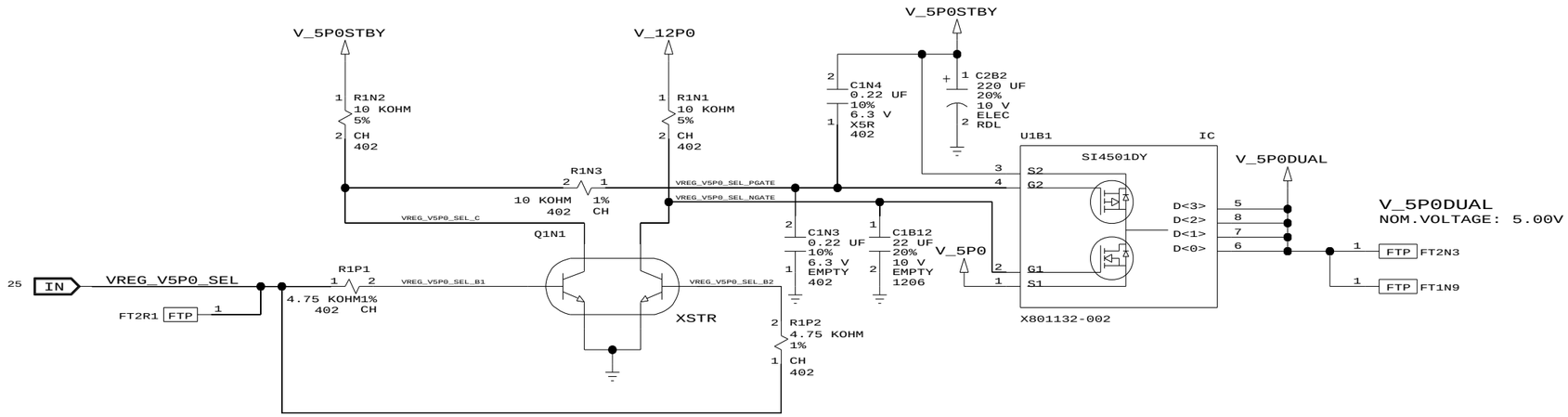
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	45/74	45/74	C	1.0

VREGS, V5P0 DUAL



VREG_5P0_SEL	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

[PAGE_TITLE=VREGS, V5P0 DUAL]

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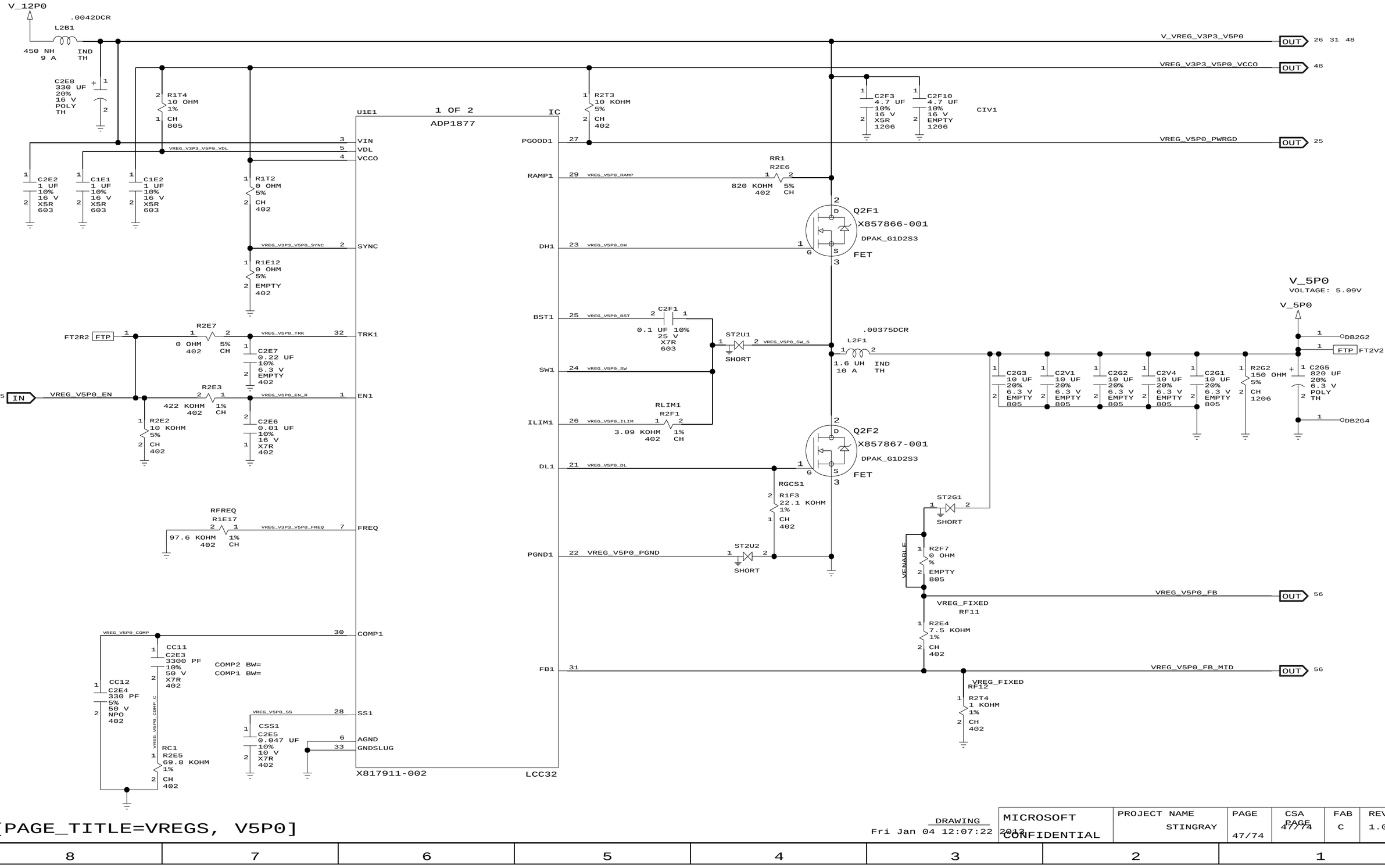
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	46/74	46/74	C	1.0

VREGS, V5P0



[PAGE_TITLE=VREGS, V5P0]

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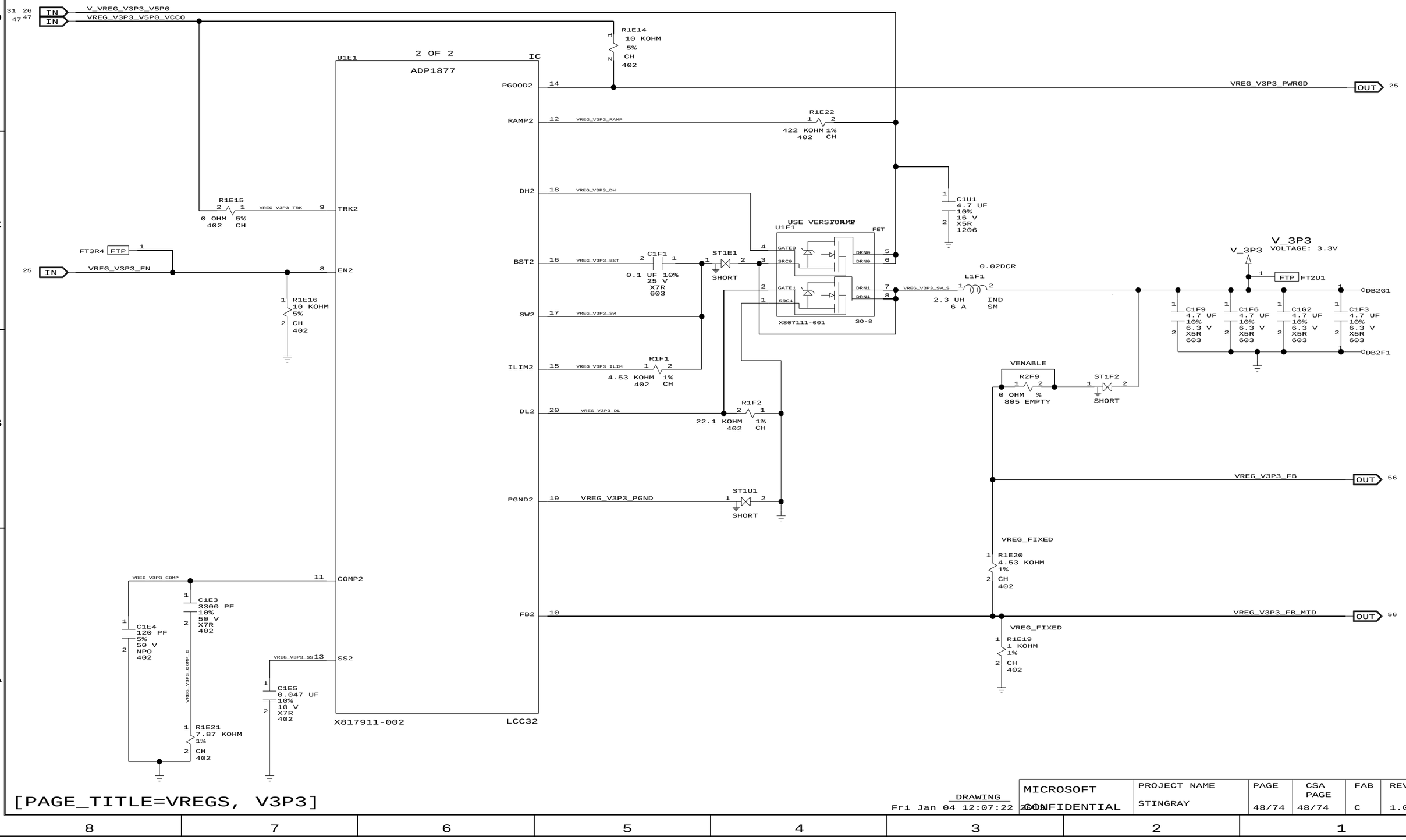
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 47/74	CSA PAGE 47/74	FAB C	REV 1.0

VREGS, V3P3



[PAGE_TITLE=VREGS, V3P3]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	48/74	48/74	C	1.0

VREGS, VEDRAM

V_12P0
.0042DCR
L7B1
450 NH
9 A
IND
TH
C3F8
330 UF
20%
16 V
POLY
TH
C7B8
470 UF
20%
16 V
POLY
TH
R3G2
10 OHM
1%
CH
805
U3G1
1 OF 2
ADP1877
IC
R3G16
10 KOHM
5%
CH
402
C3F1
4.7 UF
10%
16 V
X5R
1206
C3F7
4.7 UF
10%
16 V
EMPTY
1206
CIV1
V_VREG_VMEM_VEDRAM
OUT 50
VREG_VMEM_VEDRAM_VCCO
OUT 50
VREG_VEDRAM_PWRGD
OUT 25
VIN
VDL
VCCO
VREG_VMEM_VEDRAM_VDL
C3G1
1 UF
10%
16 V
X5R
603
C3G3
1 UF
10%
16 V
X5R
603
C3V1
1 UF
10%
16 V
X5R
603
SYNC HIGH=FORCED PWM MODE
SYNC LOW =PULSE SKIP MODE
R3F12
0 OHM
5%
CH
402
R3F14
0 OHM
5%
CH
402
VREG_VMEM_VEDRAM_SYNC
SYNC
R3F13
0 OHM
5%
EMPTY
402
VREG_VEDRAM_TRK
TRK1
PGOOD1
RAMP1
VREG_VEDRAM_RAMP
RR1
R3F10
475 KOHM
402
1%
CH
DH1
VREG_VEDRAM_DH
Q3F1
X857866-001
DPAK_G1D2S3
FET
V_CPUEDRAM
V_CPUEDRAM
VOLTAGE: 1.075V
FTP FT4T2
DB4E3
.0034DCR
L4F1
1.7 UH
13.8 A
IND
TH
C4E3
820 UF
20%
2.5 V
POLY
RDL
C4E6
820 UF
20%
2.5 V
EMPTY
RDL
C4F7
820 UF
20%
2.5 V
EMPTY
RDL
BST1
VREG_VEDRAM_BST
C3F5
0.1 UF
10%
25 V
X7R
603
ST3F1
SHORT
VREG_VEDRAM_SW_S
SW1
VREG_VEDRAM_SW
RLIM1
R3F7
3.09 KOHM
402
1%
CH
ILIM1
VREG_VEDRAM_ILIM
Q4F1
X857867-001
DPAK_G1D2S3
FET
C5T52
4.7 UF
10%
16 V
EMPTY
1206
C5E11
4.7 UF
10%
16 V
EMPTY
1206
C4T7
4.7 UF
10%
16 V
EMPTY
1206
C5E10
4.7 UF
10%
16 V
EMPTY
1206
DL1
VREG_VEDRAM_DL
RGCS1
R3V1
22.1 KOHM
1%
EMPTY
402
ST5E1
SHORT
DB4E4
DB4E5
VENABLE
R3F11
0 OHM
%
EMPTY
805
PGND1
VREG_VEDRAM_PGND
ST4U1
SHORT
VREG_VEDRAM_FB
OUT 55
VREG_FIXED
RF11
R3F8
7.87 KOHM
1%
CH
402
FB1
VREG_VEDRAM_FB_MID
OUT 55
VREG_FIXED
RF12
R3F9
10 KOHM
1%
CH
402
FT2T9 FTP
25 IN
VREG_VEDRAM_EN
EN1
R3F15
10 KOHM
5%
CH
402
RFREQ
R3G4
97.6 KOHM
402
1%
CH
VREG_VEDRAM_FREQ
FREQ
VREG_VEDRAM_COMP
COMP1
CC11
C3F2
1000 PF
10%
50 V
X7R
402
CC12
C3F3
10 PF
5%
50 V
NPO
402
VREG_VEDRAM_COMP_C
RC1
R3F6
169 KOHM
1%
CH
402
RC1=120K
VREG_VEDRAM_SS
SS1
CSS1
C3F4
0.047 UF
10%
10 V
X7R
402
AGND
GNDSLUG
X817911-002
LCC32

[PAGE_TITLE=[VREGS, VEDRAM]

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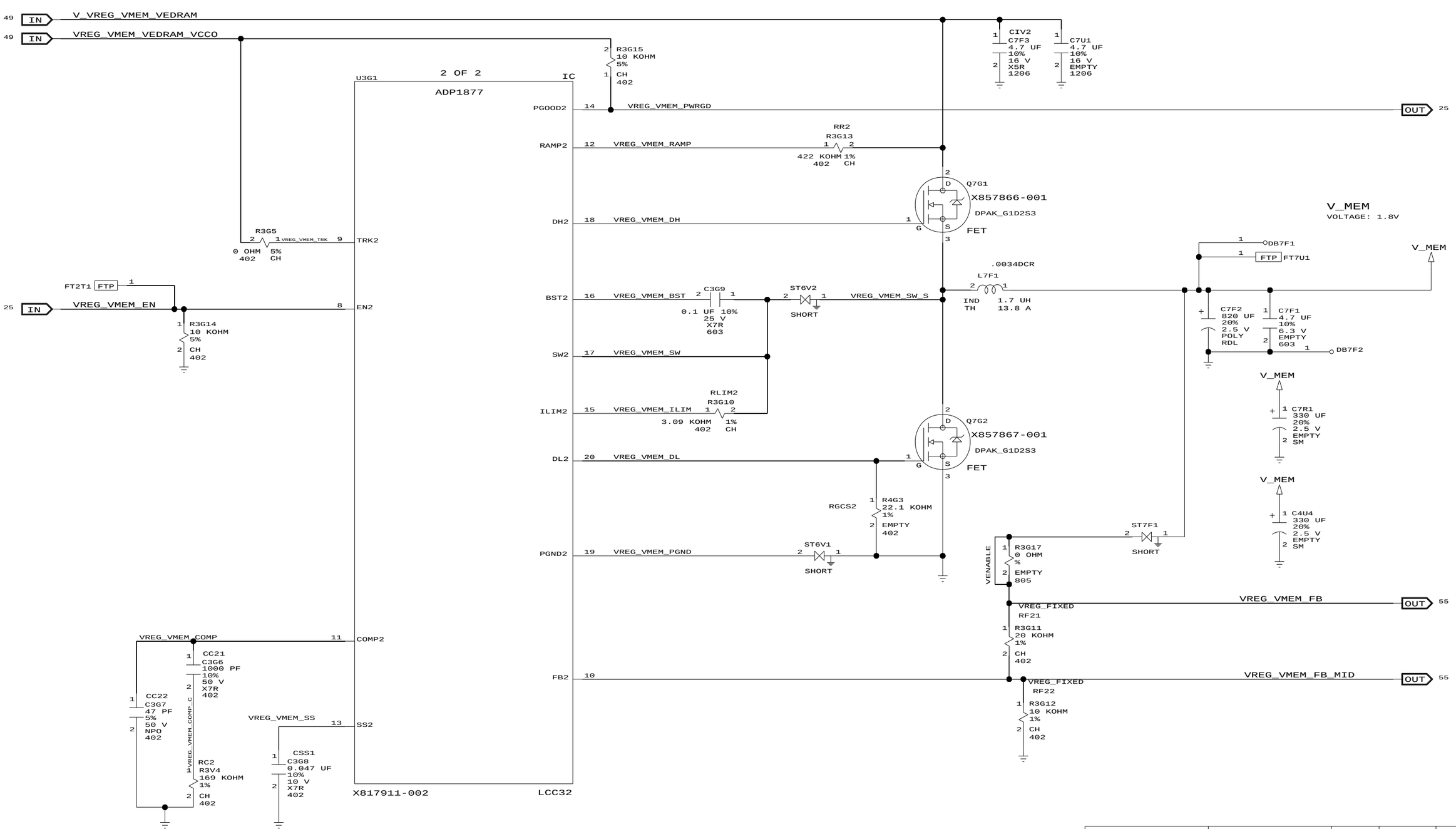
MICROSOFT	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
CONFIDENTIAL	STINGRAY	49/74	49/74	C	1.0

VREGS, VMEM

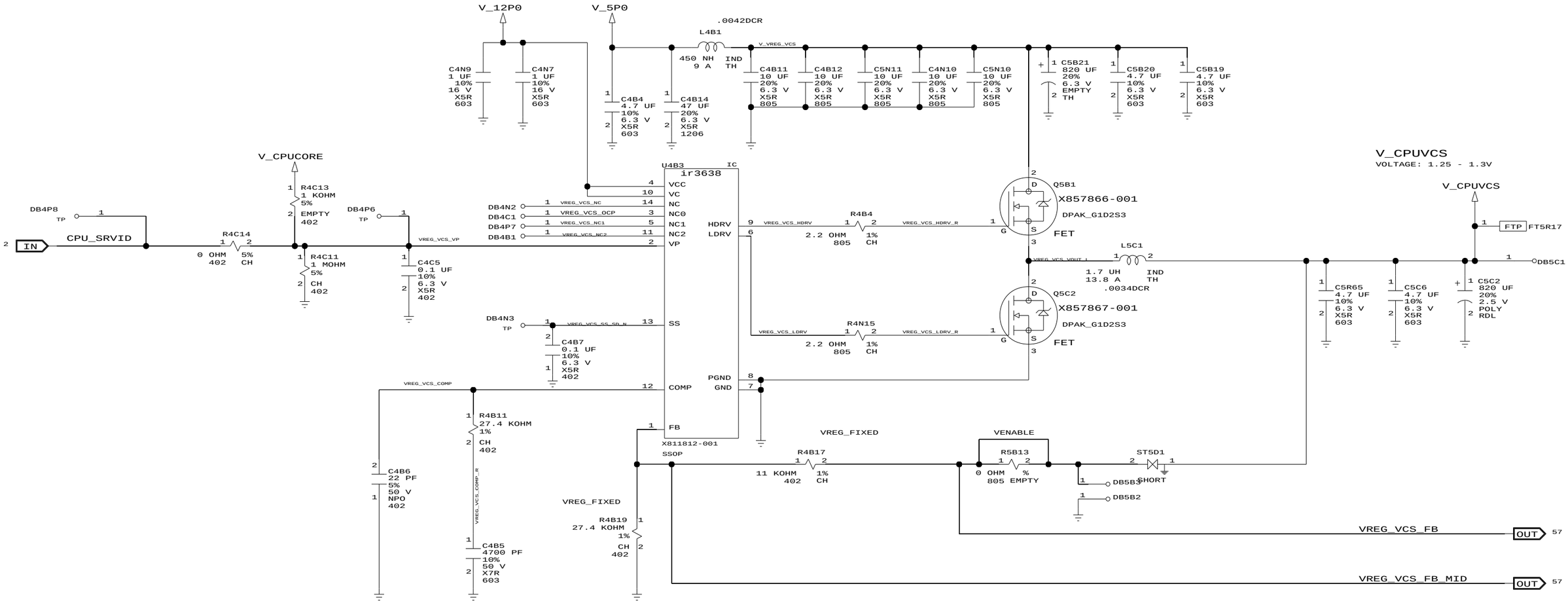


[PAGE_TITLE=[VREGS, VMEM]

DRAWING
Fri Jan 04 12:07:23 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	50/74	50/74	C	1.0

VREGS, VCS



GAIN=0.4 WITH R4B17 = 11K, R4B19 = 27.4K
OUTPUT = CPU_SRVID(1+GAIN)

[PAGE_TITLE=VREGS, VCS]

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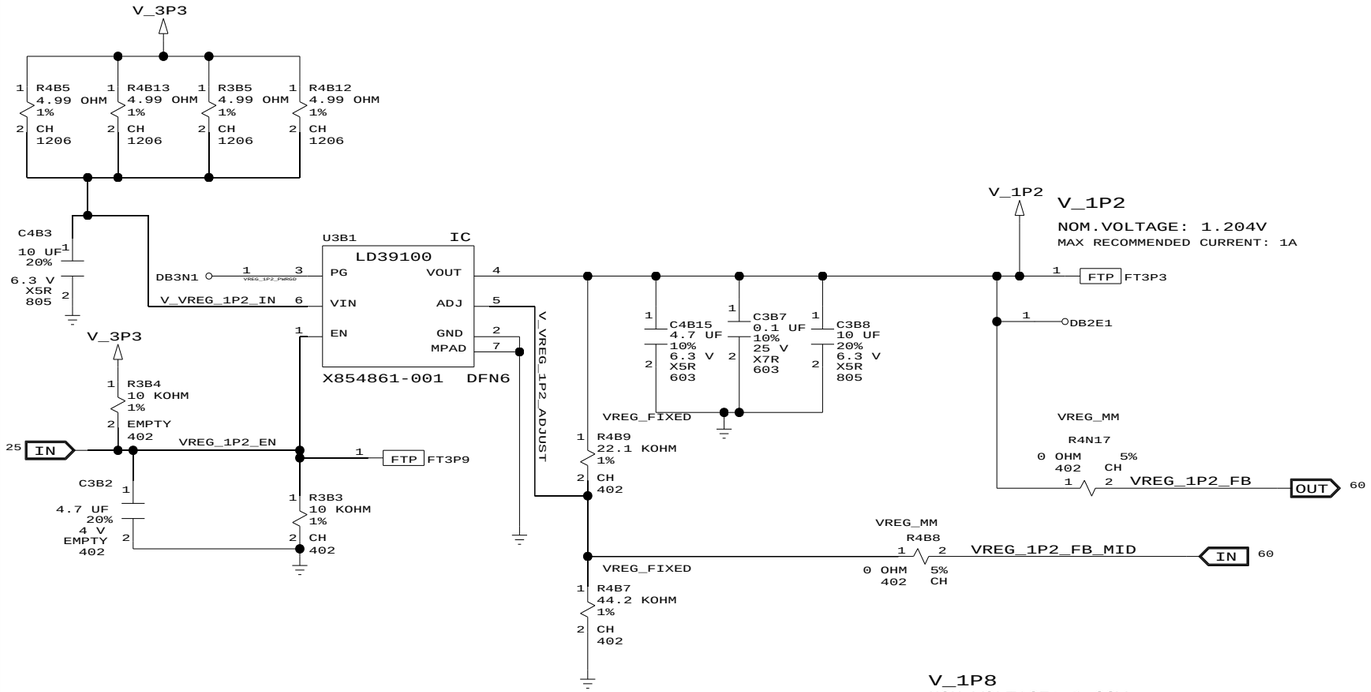
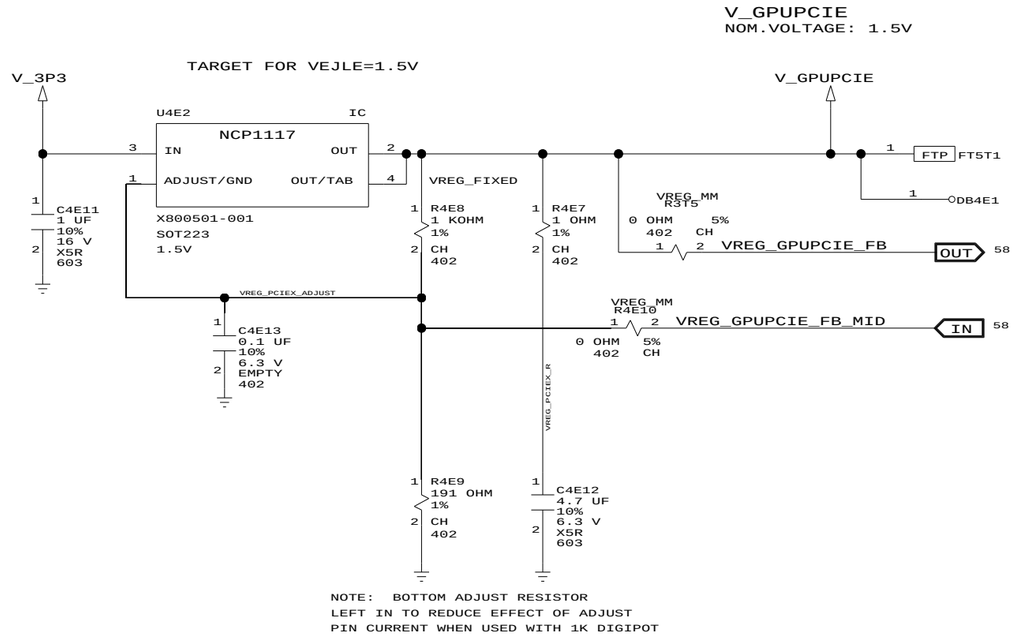
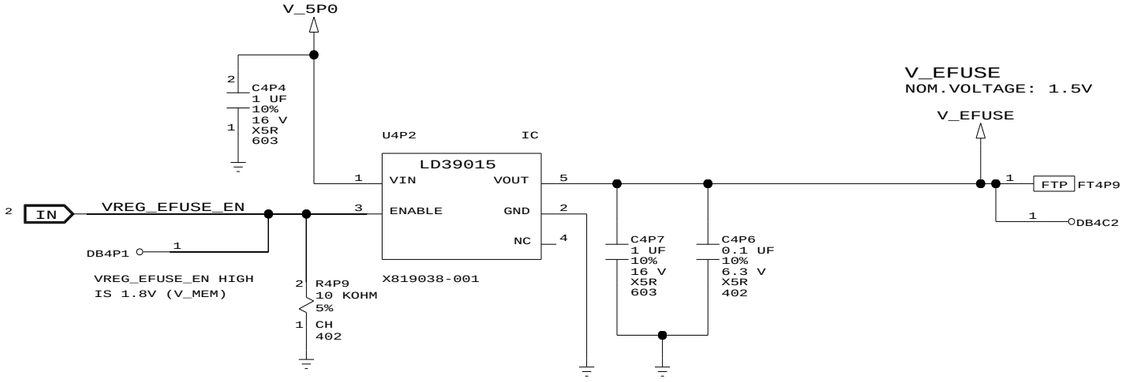
PROJECT NAME	PAGE	CSA PAGE	FAB	REV
STINGRAY	51/74	51/74	C	1.0

VREGS, 1P2+1P8+GPUPCIE+CPUPLL+EFUSE







[PAGE_TITLE=VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE]

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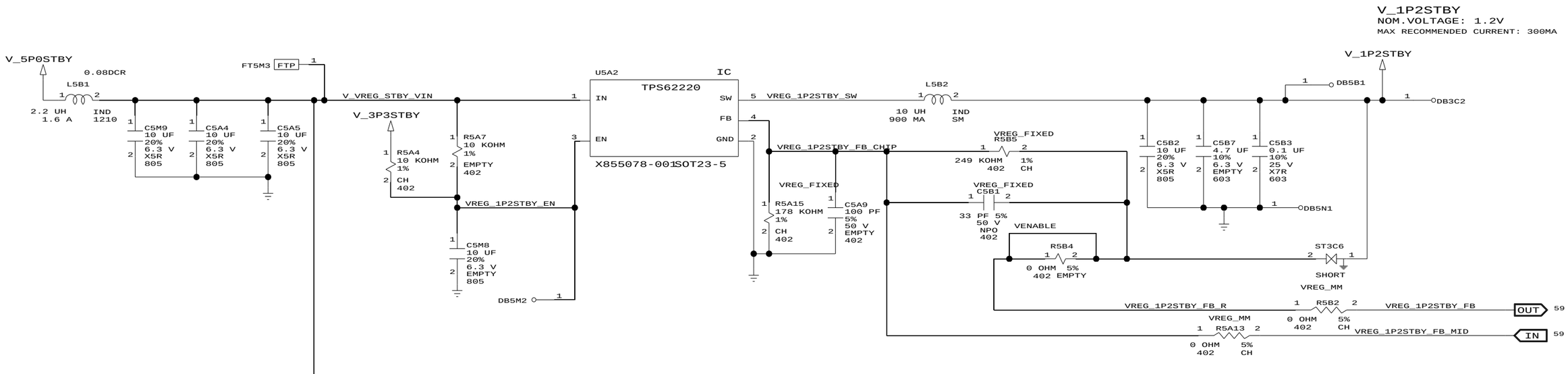
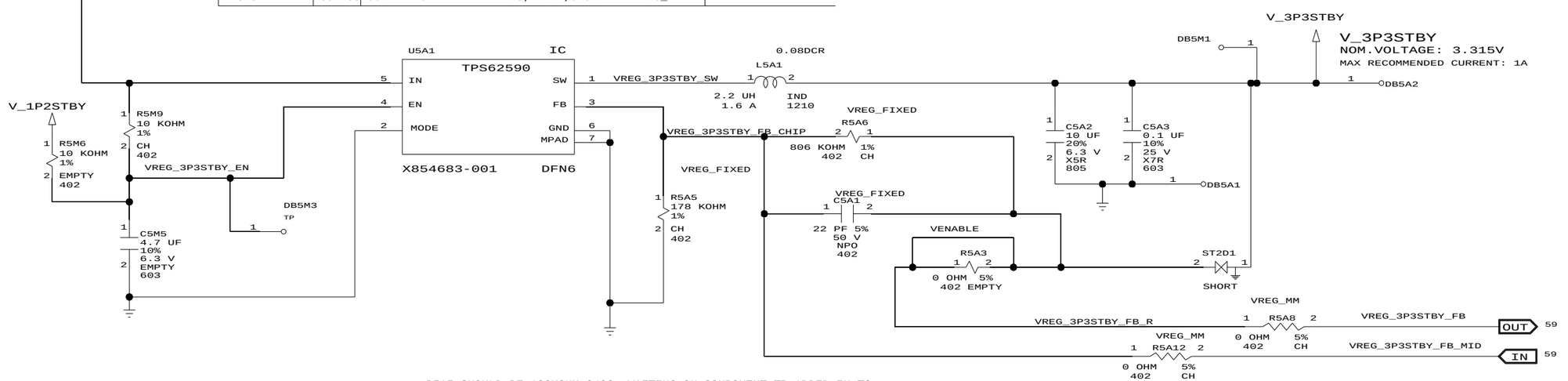
MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 52/74	CSA PAGE 52/74	FAB C	REV 1.0

VREGS, STANDBY SWITCHERS

MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R5B5	X855279-001	CH	RES,42.2K,0402	VREG_MM	PACK_IGNORE=TRUE
C5B1	X800440-001	NPO	CAP,75PF,0402	VREG_MM	PACK_IGNORE=TRUE
R5A15	X800467-001	CH	RES,30.1K,0402	VREG_MM	PACK_IGNORE=TRUE



MS_PART#	MATL	REF_DES		DESCR.	BOM PROPERTY
R5A6	X802226-001	CH	RES,100K,0402	VREG_MM	PACK_IGNORE=TRUE
C5A1	X801069-001	NPO	CAP,22PF,0402	VREG_MM	PACK_IGNORE=TRUE
R5A5	X801153-001	CH	RES,22.1K,0402	VREG_MM	PACK_IGNORE=TRUE



R5A5 SHOULD BE 182KOHM 0402, WAITING ON COMPONENT TB ADDED IN TC

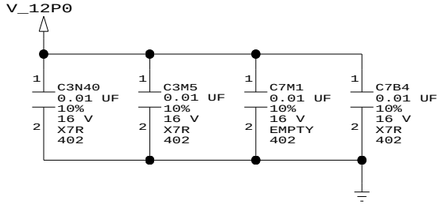
[PAGE_TITLE=VREGS, STANDBY SWITCHERS]

DRAWING
Fri Jan 04 12:07:23 2008

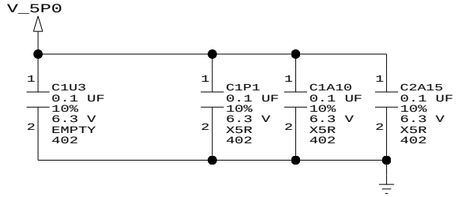
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	53/74	53/74	C	1.0

BOARD LEVEL DECOUPLING

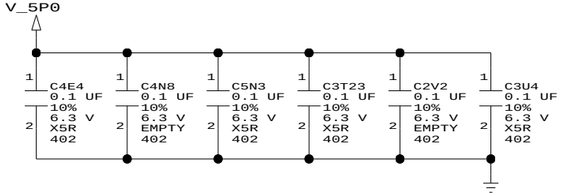
V_12P0



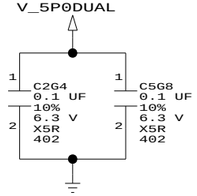
V_5P0



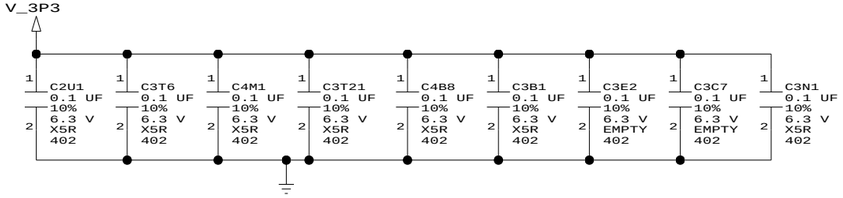
V_5P0



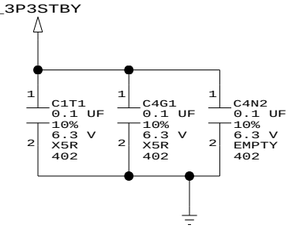
V_5P0DUAL



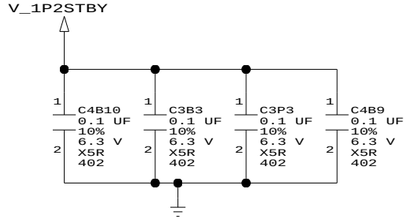
V_3P3



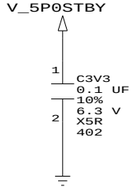
V_3P3STBY



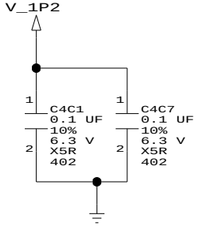
V_1P2STBY



V_5P0STBY



V_1P2

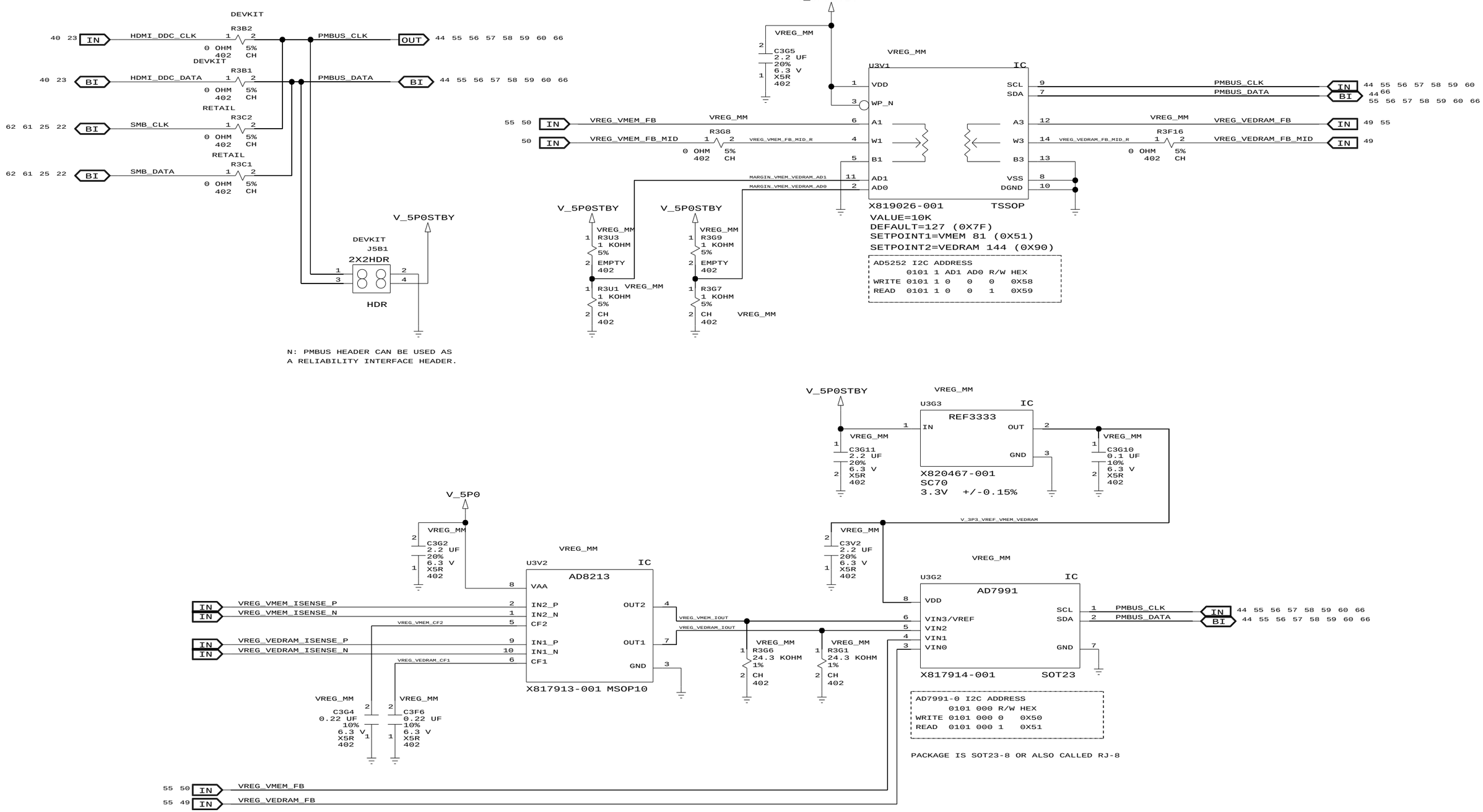


[PAGE_TITLE=BOARD, DECOUPLE]

DRAWING
Fri Jan 04 12:07:23 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	54/74	54/74	C	1.0

MARGIN, VMEM + VEDRAM

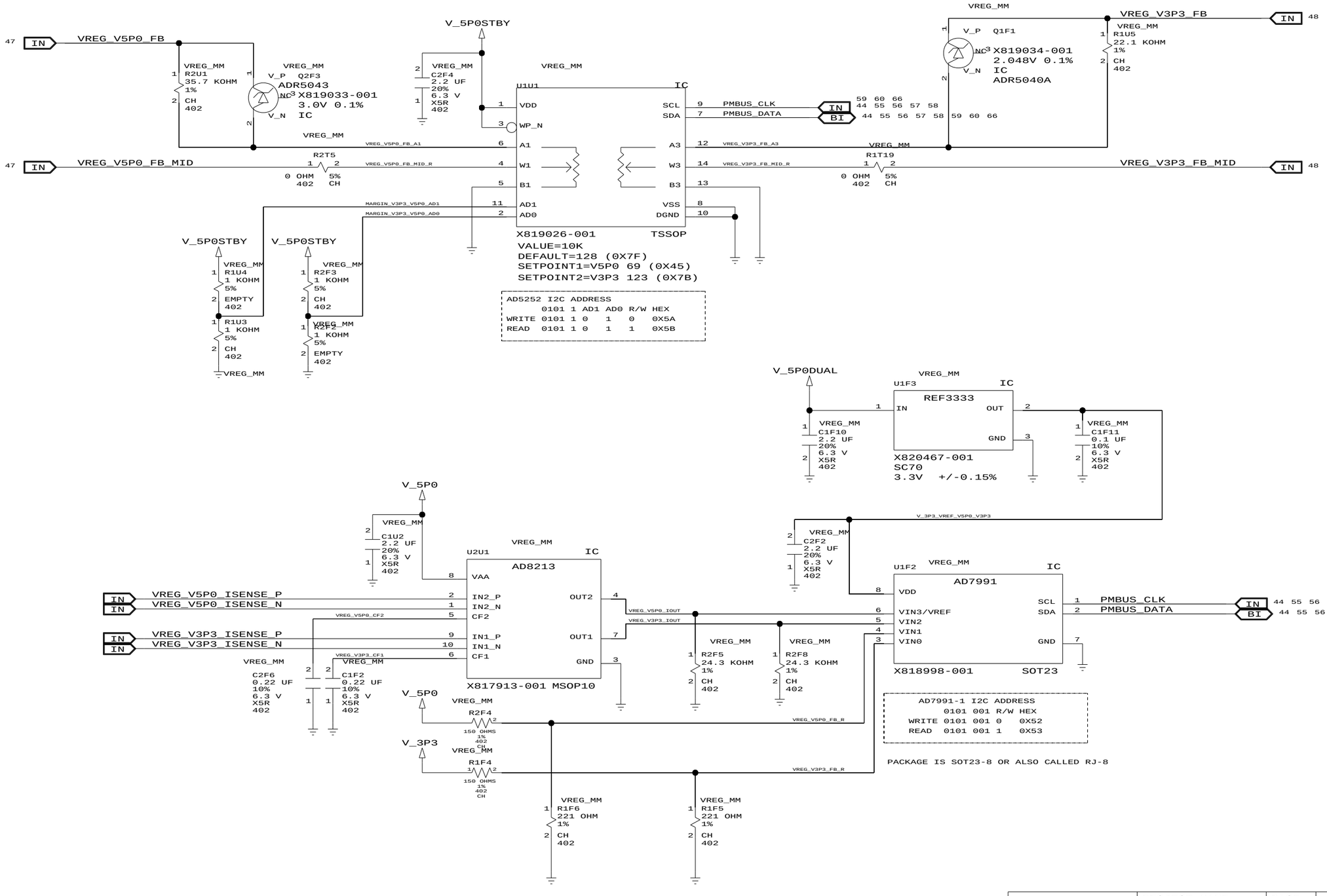


[PAGE_TITLE=MARGIN, VMEM + VEDRAM]

DRAWING
Fri Jan 04 12:07:24 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	55/74	55/74	C	1.0

MARGIN, V3P3 + V5P0



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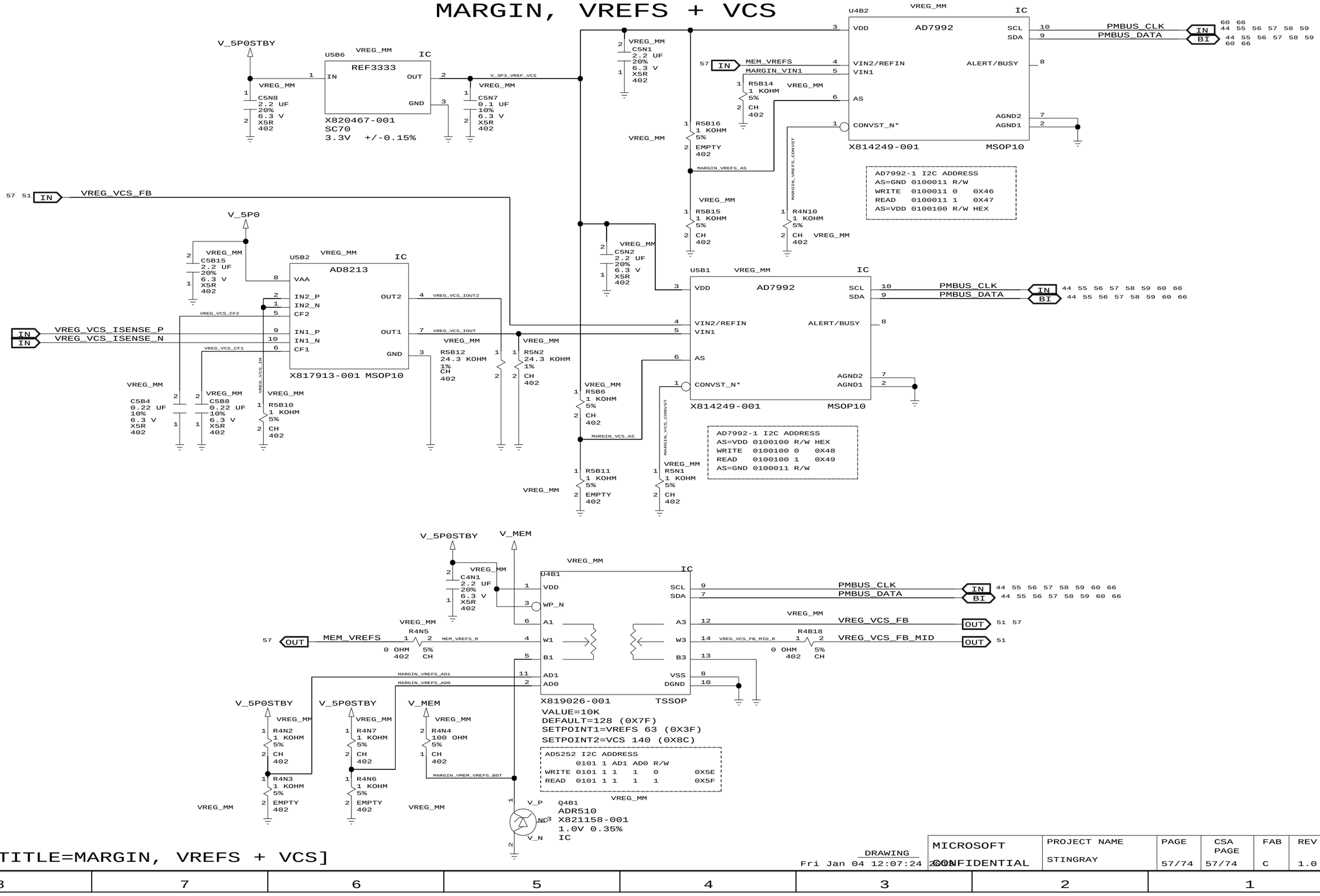
DRAWING
Fri Jan 04 12:07:24 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	56/74	56/74	C	1.0

MARGIN, VREFS + VCS

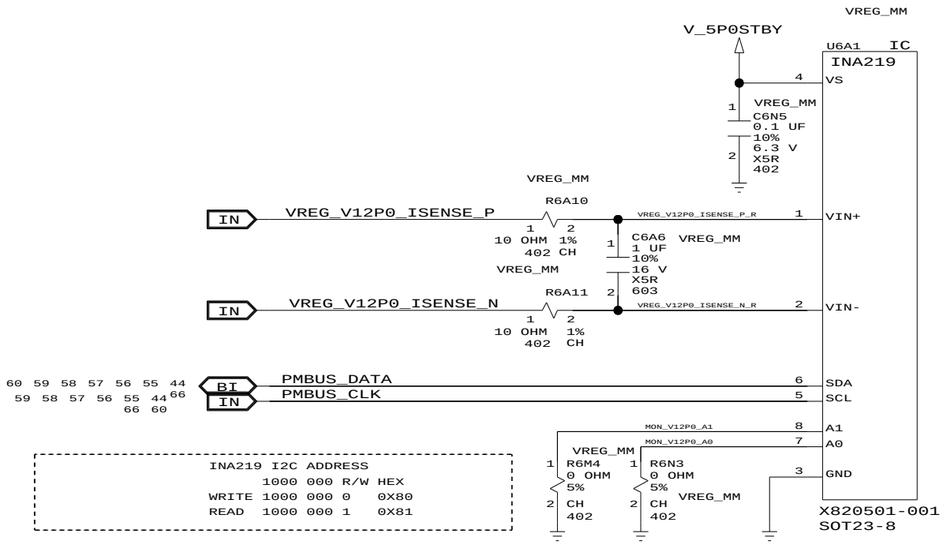


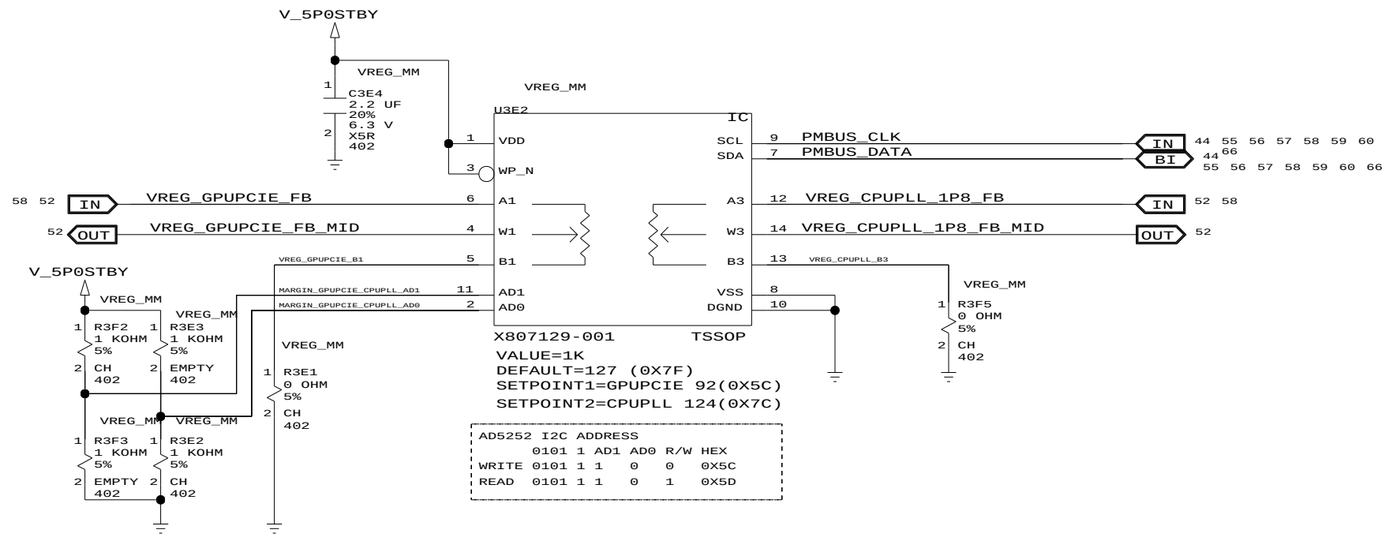
[PAGE_TITLE=MARGIN, VREFS + VCS]

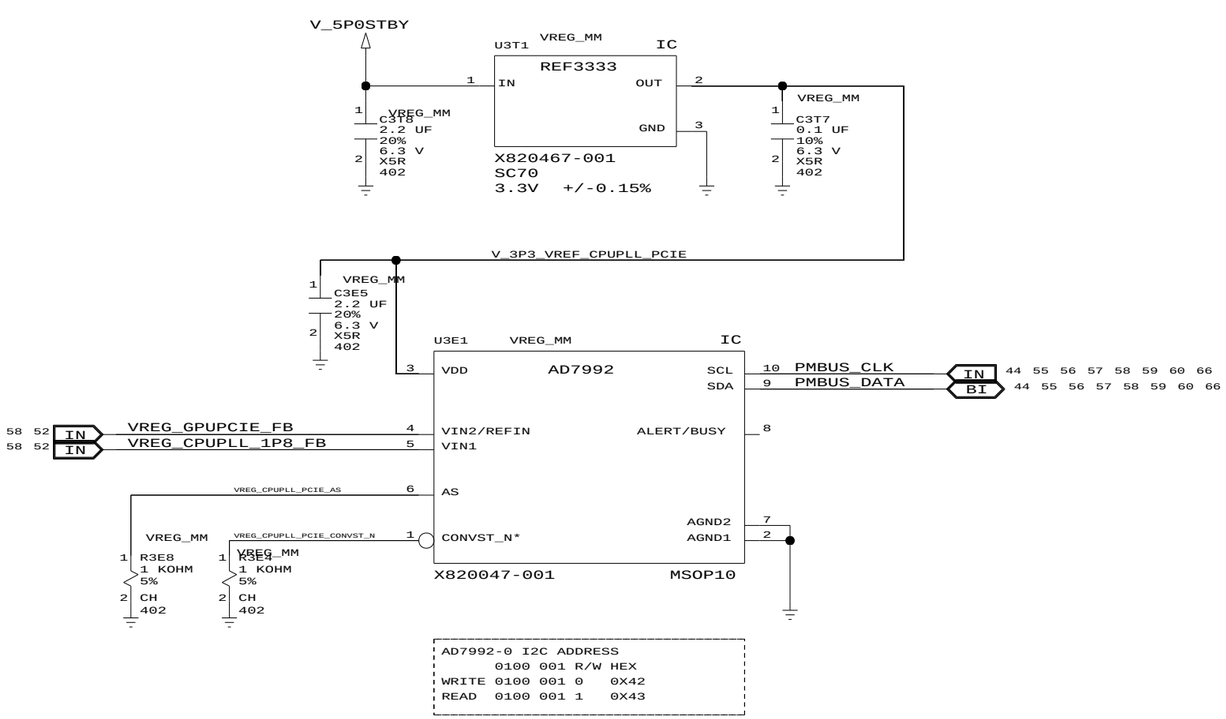
DRAWING
Fri Jan 04 12:07:24 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	57/74	57/74	C	1.0

MARGIN, VGPUPCIE,1P8, VCPUPLL, V12P0, TEMP





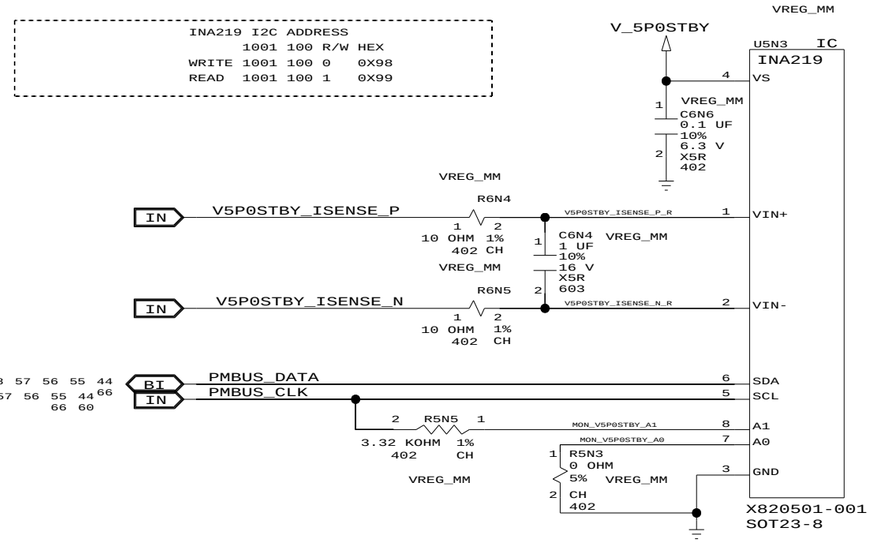


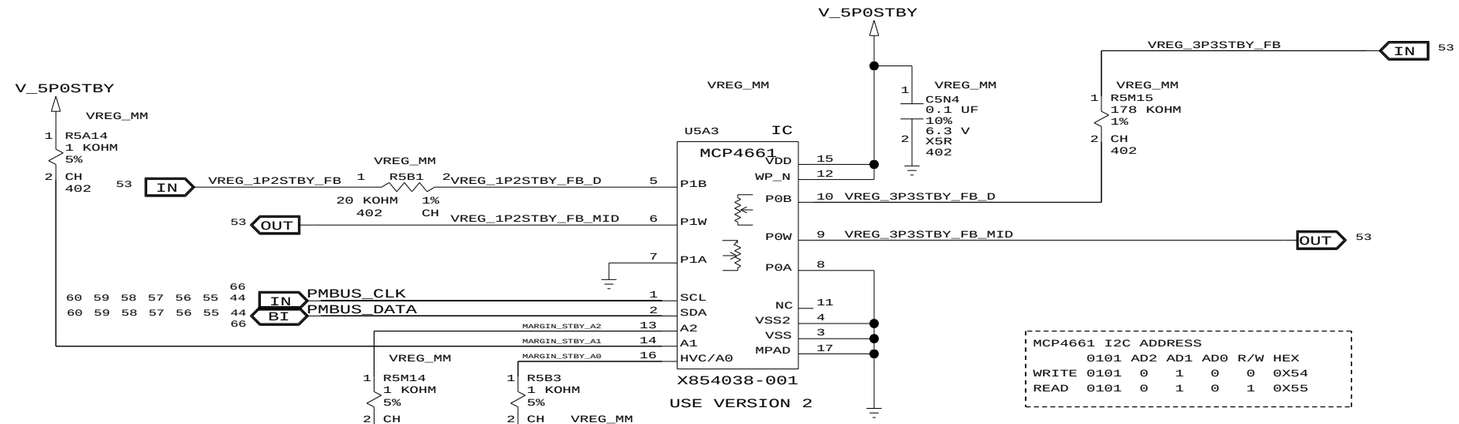
[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

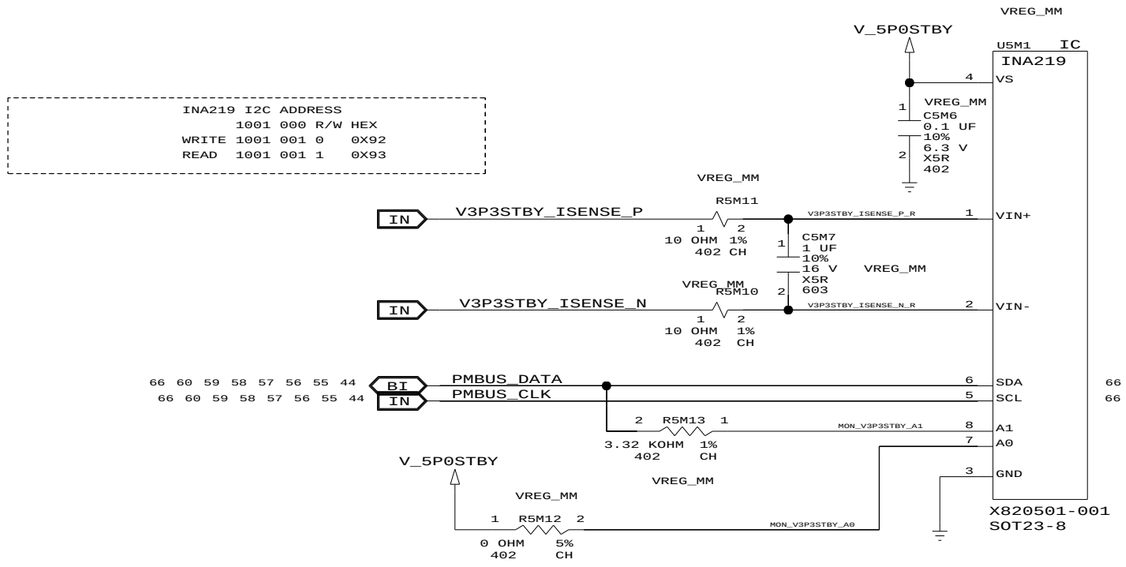
DRAWING
Fri Jan 04 12:07:24 2008

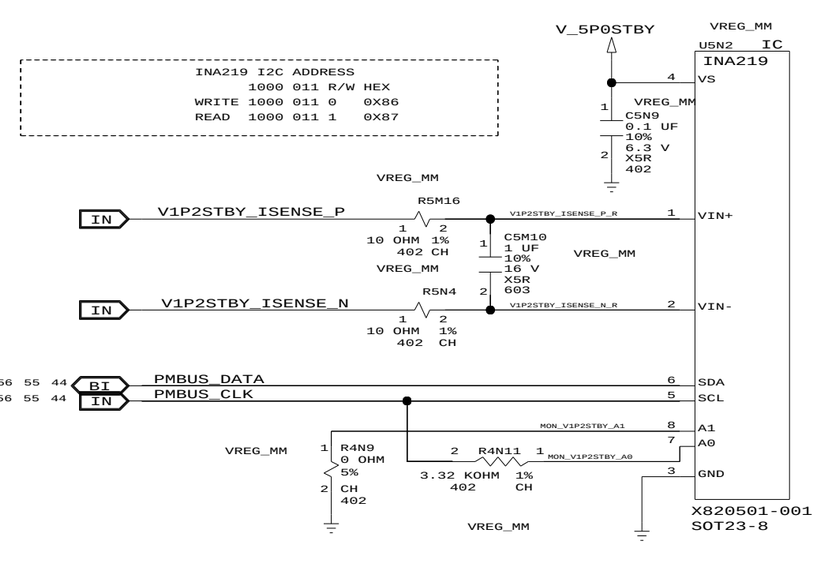
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	58/74	58/74	C	1.0

MARGIN, STANDBY







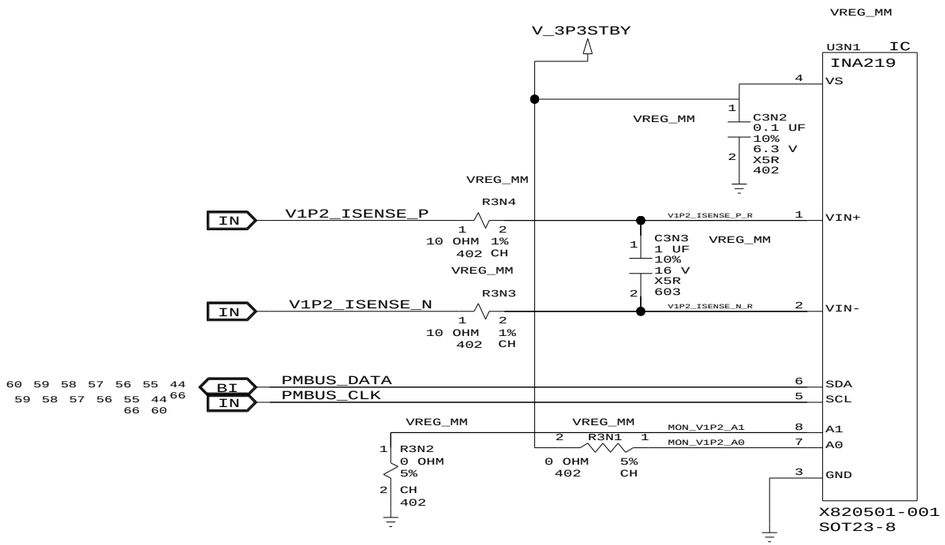


[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

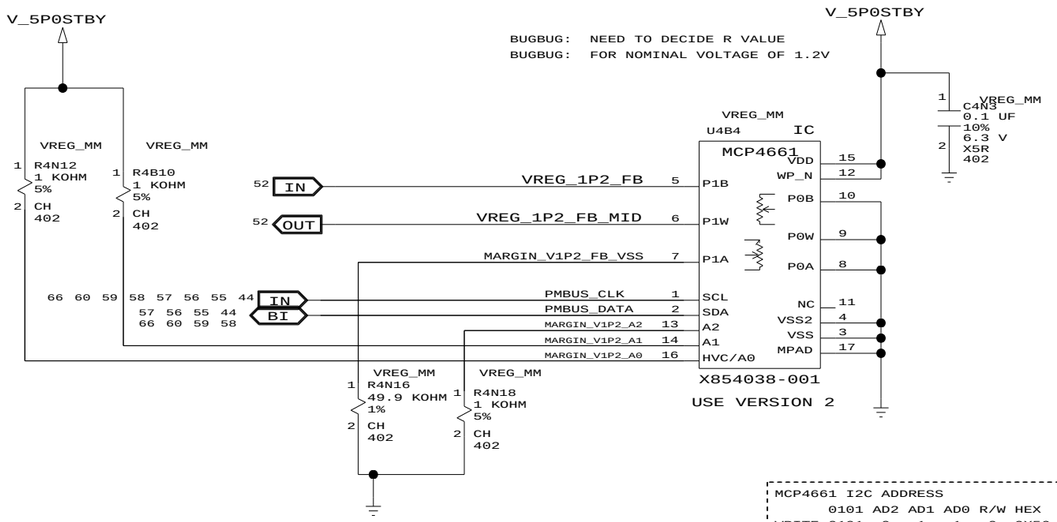
DRAWING
Fri Jan 04 12:07:25 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	59/74	59/74	C	1.0

MARGIN, V1P2



INA219 I2C ADDRESS					
	1000	100	R/W	HEX	
WRITE	1000	001	0	0X82	
READ	1000	001	1	0X83	



MCP4661 I2C ADDRESS						
	0101	AD2	AD1	AD0	R/W	HEX
WRITE	0101	0	1	1	0	0X56
READ	0101	0	1	1	1	0X57

[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

DRAWING
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PROJECT NAME	PAGE	CSA PAGE	FAB	REV
STINGRAY	60/74	60/74	C	1.0

EXTERNAL TEMP SENSORS

ISOLATE CLOSE TO KSB

62 55 25 22 BI SMB_CLK 1 R3P7 2 SMB_CLK_EXTTEMP_R 1 R3R13 2 SMB_CLK_EXTTEMP BI 61
0 OHM 5% 402 CH JTM_EXT 0 OHM 5% 402 CH JTM_EXT

62 55 25 22 BI SMB_DATA 1 R3P6 2 SMB_DATA_EXTTEMP_R 1 R3R14 2 SMB_DATA_EXTTEMP BI 61
0 OHM 5% 402 CH JTM_EXT 0 OHM 5% 402 CH JTM_EXT

ISOLATE CLOSE TO EXT TEMP

4 OUT CPU_TEMP_P — 1 R4D7 2 CPU_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23 66
1 R4R28 2 CPU_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT — OUT 61
C4D3 100 PF 5% 50 V EMPTY 402

4 OUT CPU_TEMP_N — 1 R4D8 2 CPU_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23 66
1 R4R29 2 CPU_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT

4 OUT GPU_TEMP_P — 1 R4D6 2 GPU_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23 66
1 R4R27 2 GPU_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT — OUT 61
C4D2 100 PF 5% 50 V EMPTY 402

4 OUT GPU_TEMP_N — 1 R4D5 2 GPU_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23 66
1 R4R26 2 GPU_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT

38 23 OUT BRD_TEMP_P — 1 R3R18 2 BRD_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23
1 R3D30 2 BRD_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT — OUT 61
402 EMPTY 50 V 5% C3R56 100 PF

38 23 OUT BRD_TEMP_N — 1 R3R19 2 BRD_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23
1 R3D31 2 BRD_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT

4 OUT EDRAM_TEMP_P — 1 R4D3 2 EDRAM_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23 66
1 R4R24 2 EDRAM_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT — OUT 61
C4D1 100 PF 5% 50 V EMPTY 402

4 OUT EDRAM_TEMP_N — 1 R4D4 2 EDRAM_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT — OUT 23 66
1 R4R25 2 EDRAM_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT

ST4R1 SHORT
ST4D1 SHORT
ST4R2 SHORT

61 IN CPU_TEMP_P_EXT — C4R4 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
61 IN GPU_TEMP_P_EXT — C4R5 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
61 IN BRD_TEMP_P_EXT — C4R1 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
61 IN EDRAM_TEMP_P_EXT — C4R3 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR

EXT_TEMP_N — 1 JTM_EXT R4R35 0 OHM 5% CH 402 2

JTM_EXT U4R1 IC TMP423
1 DXP1 V+ 8 — JTM_EXT C4R2 0.1 UF 10% 6.3 V X5R 402
2 DXP2 SCL 7 SMB_CLK_EXTTEMP BI 61
3 DXP3 SDA 6 SMB_DATA_EXTTEMP BI 61
4 DXN GND 5
X858059-001 SOT23-8

V_EXTTEMP

TMP423B I2C ADDRESS
1001 100 R/W HEX
WRITE 1001 101 0 0X9A
READ 1001 101 1 0X9B

V_EXTTEMP
25 IN EXT_TEMP_PWR_CTRL — 1 Q3R1 EMPTY 1.1 OHM SOT23 3 — 1 JTM_EXT R4R36 0 OHM 5% CH 402 2 — 1 FTP FT3R18
1 R3R20 10 KOHM 1% EMPTY 402 2
V_3P3STBY

V_3P3STBY
JTM_EXT C3D10 0.1 UF 10% 6.3 V X5R 402 — JTM_EXT C3D11 0.1 UF 10% 6.3 V X5R 402

STITCHING CAPS FOR BRD_TEMP PLANE SPLIT

V_EXTTEMP
61 IN EDRAM_TEMP_P_EXT — C4R3 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
JTM_EXT C3D9 0.1 UF 10% 6.3 V X5R 402

JTM_EXT U3R1 IC TMP441
1 DXP V+ 8
2 DXN SCL 7 SMB_CLK_EXTTEMP BI 61
3 A1 SDA 6 SMB_DATA_EXTTEMP BI 61
4 A0 GND 5
X858003-001 SOT23-8

EXT_TMP_A1
EXT_TMP_A0

V_EXTTEMP — JTM_EXT R4R31 0 OHM 5% CH 402 — R4R30 0 OHM 5% EMPTY 402
V_EXTTEMP — R4R33 0 OHM 5% EMPTY 402 — R4R32 0 OHM 5% JTM_EXT CH 402
1 R4R34 0 OHM 5% EMPTY 402 2

TMP441 I2C ADDRESS
10011 AD1 AD0 R/W HEX
WRITE 10011 1 0 0 0X9C
READ 10011 1 0 1 0X9D

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	61/74	61/74	C	1.0

XDK, DEBUG CONNECTORS

KSB DEBUG BUS

J2C2 EMPTY

2X13SOFTTOUCH

24	IN	FAN_TACH_SMM_R	A1	A_D1	B_D0	B1	WSS_CNTL1	IN 24 37
37 24	IN	WSS_CNTL0	A2	A_D3	B_D2	B2	SCART_RGB	IN 24 37
			A3	A_GND1	B_GND0	B3		
24	IN	SB_GPIO<4>	A4	A_D5	B_D4	B4	SB_GPIO<1>	IN 24
			A5	A_D7	B_D6	B5	SB_GPIO<0>	IN 24
			A6	A_GND3	B_GND2	B6		
24	IN	SB_GPIO<2>	A7	A_D9	B_D8	B7	SB_GPIO<3>	IN 24
24	IN	AUD_SPI_CLK_R	A8	A_D11	B_D10	B8	AUD_SPI_MOSI_R	IN 24
			A9	A_GND5	B_GND4	B9		
24	IN	AUD_RDY_BSBY_R	A10	A_D13	B_D12	B10	SB_GPIO<5>	IN 24
24	IN	AUD_SSB_R	A11	A_D15	B_D14	B11	AUD_SPI_MISO_R	IN 24
			A12	A_GND7	B_GND6	B12		
			A13	A_NC	B_CLK	B13		
			27	MH1	MH3	29		
			28	MH2	MH4	30		

X854421-001

PHY MDIO INTERFACE

NET NAME	MDIO SIGNAL
SB_GPIO<1>	PCIE MDC
SB_GPIO<0>	PCIE MDIO
SB_GPIO<2>	FPHY MDIO
SB_GPIO<3>	FPHY MDC
SB_GPIO<5>	SATA0 MDC
SB_GPIO<4>	SATA0 MDIO
AUD_SPI_MOSI_R	SATA1 MDC
AUD_SPI_CLK_R	SATA1 MDIO
WSS_CNTL0	USGBRPA MDC
WSS_CNTL1	USGBRPA MDIO
AUD_RDY_BSBY_R	USGBRPB MDC
FAN_TACH	USGBRPB MDIO

26 OUT SPI_SS_N — R2C28 0 OHM 5% 402 CH — SPI_SS_N_CONN — DEVKIT J2C1 2X5HDR10 HDR

SPI_MOSI_CONN — R2C29 0 OHM 5% 402 CH — SPI_MOSI OUT 26

26 IN SPI_MISO — 2 4 6 8 / 1 3 5 7 9

SPI_CLK_CONN — R2C30 0 OHM 5% 402 CH — SPI_CLK OUT 26

V_5P0STBY

DEVKIT C2C3 0.1 UF 10% 6.3 V X5R 402

DEVKIT J2C3 2X7HDR14 HDR

24	IN	KER_DBG_TXD	2	1
25	IN	SMC_DBG_TXD	4	3
25	OUT	SMC_DBG_EN	6	5
			8	7
		SMB_CLK_R	10	9
			12	11
				13

KER_DBG_RXD OUT 24

SMC_RST_XDK_N — R2C10 0 OHM 5% 402 CH — SMC_RST_N IN 22 25 42

V_3P3 — DEVKIT C4A12 0.1 UF 10% 6.3 V X5R 402

61 55 25 22 BI SMB_CLK — DEVKIT R2C6 100 OHM 5% 402 CH — SMB_CLK_R

V_3P3STBY

DEVKIT C2C4 0.1 UF 10% 6.3 V X5R 402

DEVKIT C2B4 1 UF 10% 16 V X5R 603

V_5P0STBY

DEVKIT C2C5 0.1 UF 10% 6.3 V X5R 402

DEVKIT C2C6 1 UF 10% 16 V X5R 603

SMB_DATA_R — DEVKIT R2C7 100 OHM 5% 402 CH — SMB_DATA BI 22 25 55 61

EXT_PWR_ON_DBG — DEVKIT R2C4 1 KOHM 5% 402 CH — EXT_PWR_ON_N OUT 25 37 65 66

[PAGE_TITLE=XDK. DEBUG CONN]

DRAWING

Fri Jan 04 12:07:25 2008

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	62/74	62/74	C	1.0

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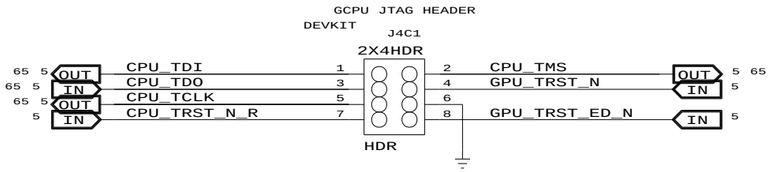
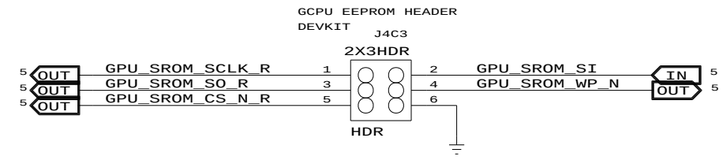
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	63/74	63/74	C	1.0

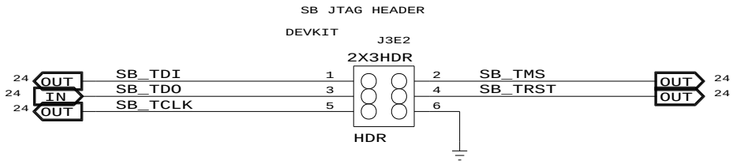
ALMOST BLANK

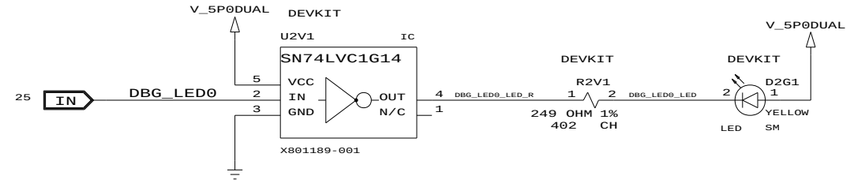
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	64/74	64/74	C	1.0

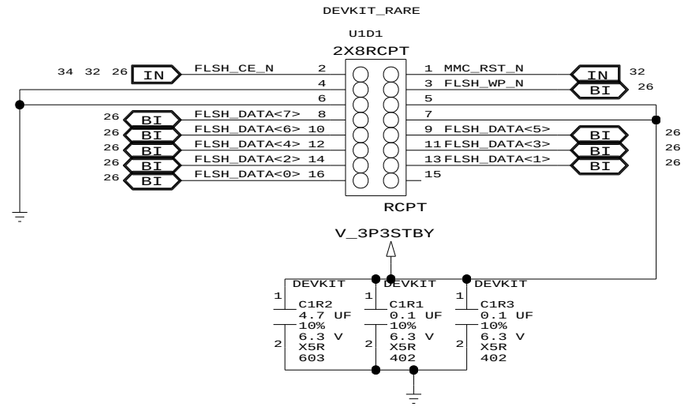
XDK DEBUG



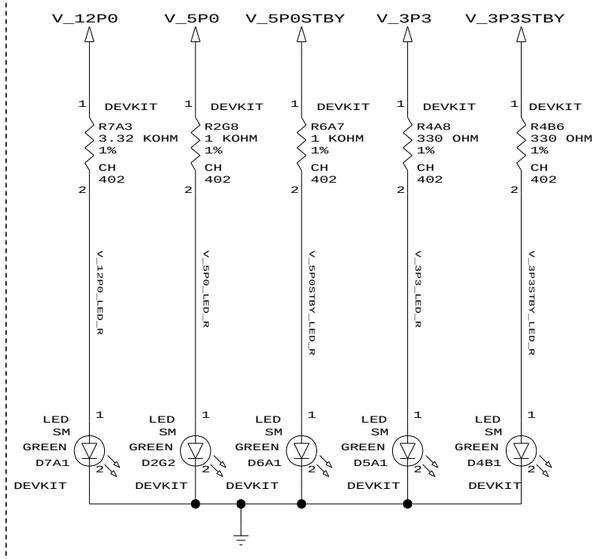








PWR LEDS



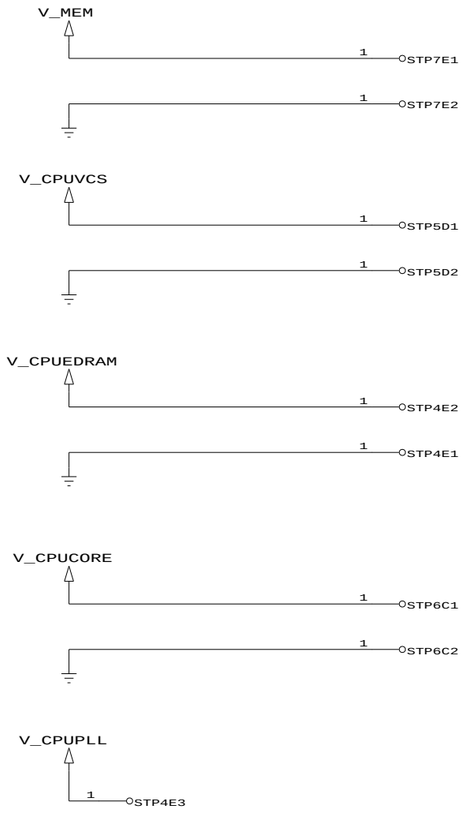
[PAGE_TITLE=XDK, DEBUG TITAN]

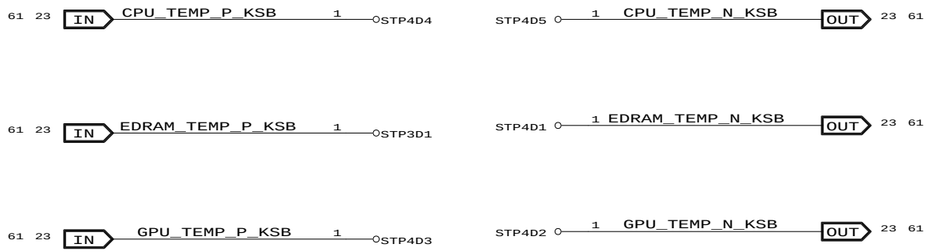
DRAWING
Fri Jan 04 12:07:26 2008

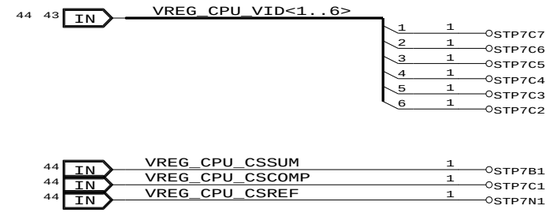
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	65/74	65/74	C	1.0

DEBUG BOARD, SPYDER CONN

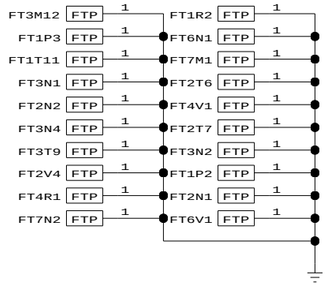
ALL STP POINTS SHALL BE ADDED TO TOP SIDE IN LAYOUT







GND FTS FOR TEST FIXTURES



[PAGE_TITLE=DEBUG BOARD, SPYDER CONN]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	66/74	66/74	C	1.0

LABELS AND MOUNTING

INTELLIGENT SERIAL NUMBER TARGET.

LB2B1
LABEL
EMPTY
X801181-001
BOM_IGNORE=TRUE

MS_PART#	MATL	REF_DES	DESCR.	BOM PROPERTY
LB2B1	X863442-001	137SX250_TARGET	LABEL,WAITSBURG	TEST

PACK_IGNORE=TRUE

X868771-001
J4A4
BOSS
SCREW-BOSS

WEST PCB MOUNTING HOLES

EDGE
MTG1B1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG1G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG4G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EAST PCB MOUNTING HOLES

EDGE
MTG7G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

HEAT SINK MOUNTING HOLES

STD
MTG4F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG4D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

[PAGE_TITLE=LABELS AND MOUNTING]

DRAWING
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PROJECT NAME	PAGE	CSA PAGE	FAB	REV
STINGRAY	67/74	67/74	C	1.0

POWER ARCHITECTURE

+12V
I=10.83A
P=130W

L1
0.4W
450nH/8A
Iin_max 5.8A
0.4W
2x470uF/
16V
Poly
10mOhm
4x4.7uF
1x1uF
MLCC
2.9A
1.62W
DPAK
1.38W
DPAK
1.15W
420nH/dual
Isat 40A
250KHz/ph
L2
1.38W
DPAK
V_CPUCORE
0.9V-1.2V
43W TD/48A TD
51.6W Max/57A Max
54A TD
Min load 20%
η=82%
0.12W
6x820uF/
2.5V
Poly
7mOhm
2.9A
1.62W
DPAK
1.15W
L2
1.38W
DPAK
1.38W
DPAK

+5POSTBY
I=1.0A
P=5W
0.09W
2.2uH
Iin_max 0.91A
V_5P0DUAL
1.5A TD
8.4W Max
DUALSO8
7W
3x10uF/
6.3V
MLCC
8mOhm
1x0.1uF/
16V
MLCC
xmOhm
0.06A
SOT23-5
0.24W
0.1W
2.2uH/
1.7MHz
Isat 1.3A
1x10uF/
6.3V
MLCC
8mOhm
V_1P2STBY
0.20W TD/0.15A TD
0.24W Max/0.20mA Max
η=85%
V_EFUSE
0.02A TD
0.03W TD
V_EFUSE(1.5V)
Linear SOT23
0.08W Max
Measured data shows
v_3p3 may be 330mA
less than budget
0.66A
SOT23-5
0.4W
0.08W
2.2uH/
1.7MHz
Isat 0.9A
1x10uF/
6.3V
MLCC
8mOhm
V_3P3STBY
2.1W TD/0.64A TD
2.64W Max/0.80A Max
η=85%
L1
0.12W
450nH/8A
Iin_max 3.4A
3x4.7uF/
6.3V
MLCC
11mOhm
2x1uF/
6.3V
MLCC
0.5W
DPAK
1.21W*
(0.81W)
DPAK
L3
1.4W
1.7uH/
400KHz
Ipk 12.4A
820uF/
2.5V
Poly
7mOhm
V_VCS
1.25-1.3V
12W TD/9.6A TD
13.2W Max/10.6A Max
η=82%
1.0 Ohm/
0.0625W
each, 0402
V_1P2
Linear DPAK
1.08W MAX
V_1P2
0.76A TD
0.9W TD
FB
V_5P0
5.09V,
43.3W TD/ 8.1A TD
47.6W Max/ 8.9 A
Max
Min load 50%
η=93%
0.91A
V_3P3
3.3V
2.88A TD
9.5W TD
10.56W Max
Min load 50%
η=88%
V_CPUPLL
0.45A TD
0.83W TD
V_1P83PLL
Linear DPAK
1.01W Max(loss)
V_1P83 Main
0.031A TD
0.057W TD
L1
0.26W
450nH/8A
Iin_max 5.51A
0.18W
1x470uF/
16V
Poly
10mohm
4.6A
1.4W
DPAK
1.4W
1.6uH 600KHz
Ipk 13A
1x4.7uF
1x0.1uF
MLCC
1.3W*
(1.05W)
DPAK
L3
0.25W
820uF/
6.3V
E-Al
11mOhm
DUALSO8
1W
0.13W
2.3uH/600KHz
Isat 5.6A
L4
4x4.7uF/
6.5V
MLCC
8mohm
V_GPUPCIE
0.11A TD
0.165W TD
V_GPUPCIE(VTT)
(1.5V)
Linear SOT223
0.22W Max(loss)

MICROSOFT CONFIDENTIAL
CORONA XDK MB POWER ARCHITECTURE
MAX PWR4 DISSIPATION(+10% LOAD)
JAN 12, 2010

Legend
- Power rail from Switching Regulator
- Power rail from External PSU
- Power rail from Linear Regulator

0.91W*
*=using same FET like HS

Expected
Airflow=0.3m/s

L1
0.16W
450nH/8A
Iin_max 3.1A
0.19W
1x470uF/
16V
Poly
10mohm
1x330uF/
16V
Poly
10mohm
1.25A
4x4.7uF
1x1uF
MLCC
0.98W
DPAK
1.5W*
(1W)
DPAK
L3
1.2W
1.7uH/600KHz
Isat 11A
2x820uF/
2.5V
Poly
7mohm
Option
1x820uF/
2.5V
Poly
7mohm
V_EDRAM
1.075V
9.7W TD/9A TD
10.6W Max/9.9A Max
Min load 50%
η=88%
1.9A
1W
DPAK
1.4W*
(1W)
DPAK
1.2W
1.7uH/600KHz
Isat 11.5A
L3
1x820uF/
2.5V
Poly
7mohm
Option
2x330uF
OsCon
7mOhm
Option
8x10uF
MLCC
11mOhm
V_MEM
1.8V
16W TD/9A
17.8W Max/10A max
Min load 50%
η=84%

= No Change from Trinity, Regression Testing Only

= Change/New, Needs Special Attention on Corona

= Alternate Part Stuffing

Corona System

Rev 0.55, 4/16/10

HDMI

TOSLINK

AVIP

TMDS

S/PDIF

DDC

Analog Video

I2S

Audio DACs

SMBus

PHY

HDMI

DACs

PLLs

DVE

JTM

Clocks to CGPU

DVO

Board R-Cal

Thermal diode info 3

PCI-Express Bitrate: 2.5 Gbps

2

2

PCI-Express PHY

RJ-45

PHY

Ethernet

AUX Port

Expansion Port Interface (x3)

USB 2.0

USB 2.0

PHY

EHCI

OHCI

USB Group A

Controller Port Interface (x2)

Spare

USB 2.0

USB 2.0

Wave 802.11n

USB 2.0

USB 2.0

PHY

EHCI

OHCI

USB Group B

Southbridge

SATA PHY

SATA

Internal HDD

SATA PHY

SATA

ODD Drive

SMM

24

Parallel Debug

Serial

IR

SMC

GPIOs

SFC (NAND /MMC)

Capacitive Touch

FPBus

2

ROL

Radio

Baseband

Boron

5

Audio Chip

Internal Speaker

System Control, DVD Tray

Serial

SMBus

PWM Fan

8

8

16 MB NAND System Flash

SMC: 16 kB
Kernel: 1 MB
Config: 256B
Dash: < 7 MB

Phison MMC Controller

4 GB NAND Flash

Host Core

32 kB L1 I$
32 kB L1 D$

Dataflow Cores

32 kB L1 I$
32 kB L1 D$

1 MB Shared L2$

64 kB Boot ROM

3D Core (GPU)

10 MB emDRAM

Production Fuses

CGPU

18

Parallel Debug

JTAG

Serial Debug

POST

5

Debug Input

SPI

SROM

1 Gb, x32

64

1 Gb, x32

64

110 / 220 AC

External PSU

12V @ 130W
5V @ 5W
62% eff @ 1/2W

Power Delivery

V_CPUCORE 55.7A @ APSV
V_CPUEDRAM 7.3A @ 1.075V
V_CPUVCS 10.3A @ 1.25V
V_MEM 6A @ 1.8V
V_5P0 7A @ 5.09V
V_3P3 3.2A @ 3.3V
V_CPUPLL 0.6A @ 1.8V
V_3P3STBY 0.8A @ 3.3V
V_1P2STBY 0.2A @ 1.2V
V_EFUSE 0.020A @ 1.5V
V_1P2 0.9A @ 1.2V
V_GPUPCIE 0.2A @ 1.5V

Software

SMC

HWInit

Kernel

Mechanicals

Vejle HS+Fan

Minor tweaks

Plastics/ Ind Des

KSB Heatsink

Value SKU

16MB Flash will be replaced with 4GB/8GB flash using new MMC interface on KSB.

KSB

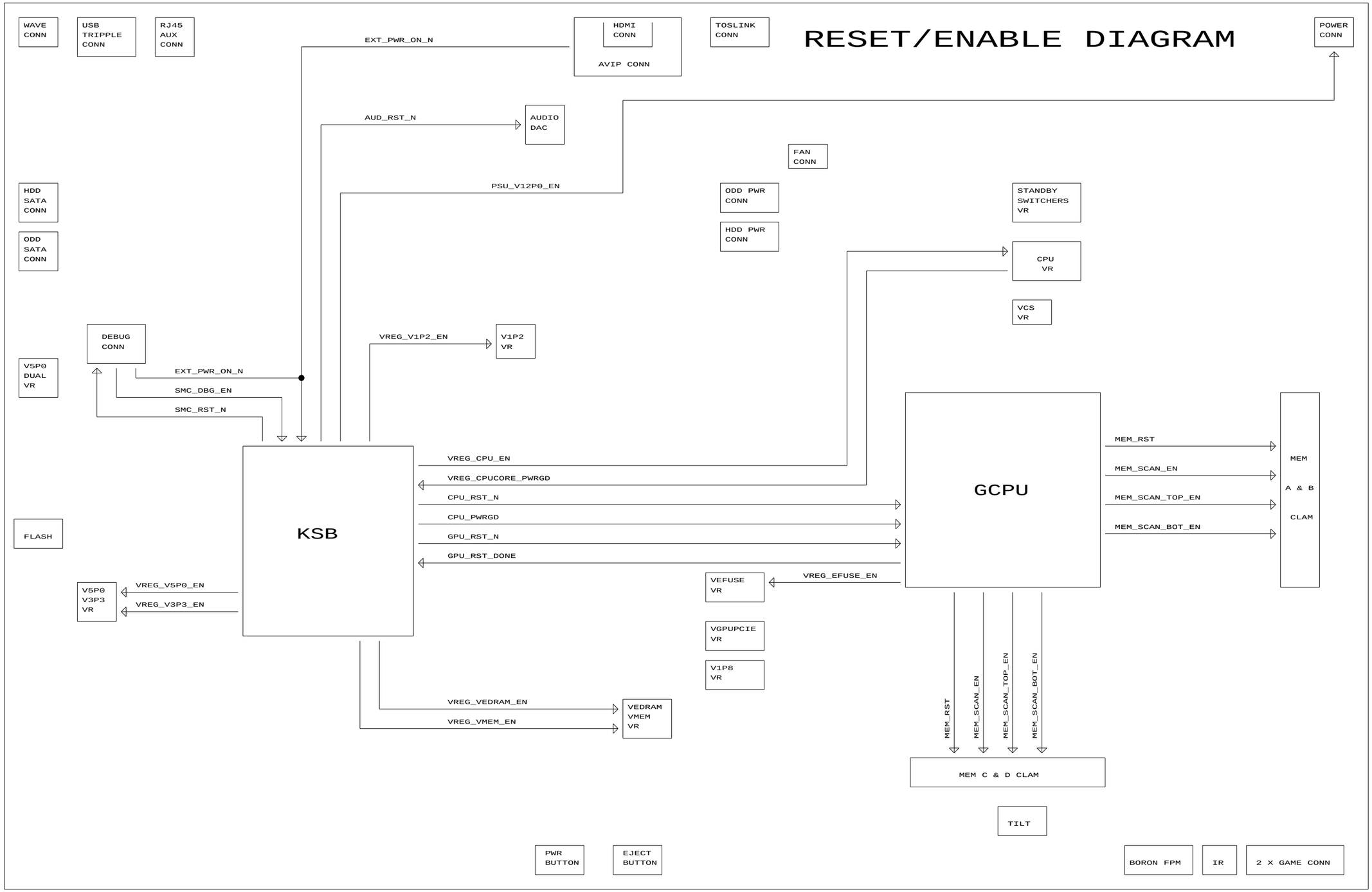
Process: 0.15u
Die Size: ~43mm^2
Frequency: 150-250 MHz
Core VDD: 1.2V
PD Power: 4W
Signal I/O: 212
Package: 23mm x 23mm 404 pin PBGA

MS Confidential

<PAGE_TITLE=SYSTEM BLOCK DIAGRAM>

DRAWING							
TRINITY_FAB_A Fri Jan 04 12:07:26 2013	MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 69/74	CSA PAGE 69/74	FAB C	REV 1.0

RESET/ENABLE DIAGRAM



<PAGE_TITLE=CLOCK DIAGRAM>

DRAWING
TRINITY_FAB_A
Fri Jan 04 12:07:27 2013

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	CSA PAGE	FAB	REV
	STINGRAY	70/74	70/74	C	1.0

COMPONENT STUFFING TABLES

MARGIN REF DES TO STUFF

REFDES	DBG/XDK	RETAIL
C1F2	STUFF	NO-STUFF
C1F10	STUFF	NO-STUFF
C1F11	STUFF	NO-STUFF
C1G7	STUFF	NO-STUFF
C1G8	STUFF	NO-STUFF
C1G9	STUFF	NO-STUFF
C1G10	STUFF	NO-STUFF
C1G11	STUFF	NO-STUFF
C1G12	STUFF	NO-STUFF
C1G13	STUFF	NO-STUFF
C1U2	STUFF	NO-STUFF
C2F2	STUFF	NO-STUFF
C2F4	STUFF	NO-STUFF
C2F6	STUFF	NO-STUFF
C2E4	STUFF	NO-STUFF
C2E5	STUFF	NO-STUFF
C2F6	STUFF	NO-STUFF
C3G11	STUFF	NO-STUFF
C3G2	STUFF	NO-STUFF
C3G4	STUFF	NO-STUFF
C3U2	STUFF	NO-STUFF
C3U3	STUFF	NO-STUFF
C3V2	STUFF	NO-STUFF
C4B1	STUFF	NO-STUFF
C4N1	STUFF	NO-STUFF
C4N4	STUFF	NO-STUFF
C5B15	STUFF	NO-STUFF
C5B5	STUFF	NO-STUFF
C5B8	STUFF	NO-STUFF
C5N7	STUFF	NO-STUFF
C5N8	STUFF	NO-STUFF
C6A6	STUFF	NO-STUFF
C6M5	STUFF	NO-STUFF
J1G3	STUFF	NO-STUFF
Q1F1	STUFF	NO-STUFF
Q2F3	STUFF	NO-STUFF
Q4B1	STUFF	NO-STUFF
R1F4	STUFF	NO-STUFF
R1F5	STUFF	NO-STUFF
R1F6	STUFF	NO-STUFF
R1G1	STUFF	NO-STUFF
R1T19	STUFF	NO-STUFF
R1U3	STUFF	NO-STUFF
R1U4	STUFF	NO-STUFF

MARGIN CONTINUED...

REFDES	DBG/XDK	RETAIL
R1U5	STUFF	NO-STUFF
R2B1	STUFF	NO-STUFF
R2B3	STUFF	NO-STUFF
R2F2	STUFF	NO-STUFF
R2F3	STUFF	NO-STUFF
R2F4	STUFF	NO-STUFF
R2F5	STUFF	NO-STUFF
R2F8	STUFF	NO-STUFF
R2T5	STUFF	NO-STUFF
R2U1	STUFF	NO-STUFF
R3E1	STUFF	NO-STUFF
R3E2	STUFF	NO-STUFF
R3E3	STUFF	NO-STUFF
R3E4	STUFF	NO-STUFF
R3F16	STUFF	NO-STUFF
R3F2	STUFF	NO-STUFF
R3F3	STUFF	NO-STUFF
R3F5	STUFF	NO-STUFF
R3G1	STUFF	NO-STUFF
R3G6	STUFF	NO-STUFF
R3G7	STUFF	NO-STUFF
R3G8	STUFF	NO-STUFF
R3G9	STUFF	NO-STUFF
R3N6	STUFF	NO-STUFF
R3U1	STUFF	NO-STUFF
R3U2	STUFF	NO-STUFF
R3U3	STUFF	NO-STUFF
R4B1	STUFF	NO-STUFF
R4B18	STUFF	NO-STUFF
R4B2	STUFF	NO-STUFF
R4B3	STUFF	NO-STUFF
R4N1	STUFF	NO-STUFF
R4N10	STUFF	NO-STUFF
R4N13	STUFF	NO-STUFF
R4N14	STUFF	NO-STUFF
R4N2	STUFF	NO-STUFF
R4N3	STUFF	NO-STUFF
R4N4	STUFF	NO-STUFF
R4N5	STUFF	NO-STUFF
R4N7	STUFF	NO-STUFF
R4N8	STUFF	NO-STUFF
R5B6	STUFF	NO-STUFF
R5N2	STUFF	NO-STUFF
R6A10	STUFF	NO-STUFF

MARGIN CONTINUED...

REFDES	DBG/XDK	RETAIL
R6A11	STUFF	NO-STUFF
R6M3	STUFF	NO-STUFF
R6M4	STUFF	NO-STUFF
U1F2	STUFF	NO-STUFF
U1F3	STUFF	NO-STUFF
U1G2	STUFF	NO-STUFF
U1U1	STUFF	NO-STUFF
U2U1	STUFF	NO-STUFF
U3E1	STUFF	NO-STUFF
U3E2	STUFF	NO-STUFF
U3G2	STUFF	NO-STUFF
U3G3	STUFF	NO-STUFF
U3T1	STUFF	NO-STUFF
U3V1	STUFF	NO-STUFF
U4B1	STUFF	NO-STUFF
U4B2	STUFF	NO-STUFF
U5B2	STUFF	NO-STUFF
U5B6	STUFF	NO-STUFF
U5N1	STUFF	NO-STUFF
U6A1	STUFF	NO-STUFF

PLEASE SEE BOM VARIANTS FOR STUFFING INSTUCTIONS ON V1P2 AND STBY MARGINING

GDDR MEM. REFDES TO STUFF

REFDES	TOP ONLY (4GB)	TOP & BOT (8GB)
C5F1	STUFF	STUFF
C5U9	STUFF	STUFF
C6F3	STUFF	STUFF
C6U7	STUFF	STUFF
C7D12	STUFF	STUFF
C7E9	STUFF	STUFF
C7R6	STUFF	STUFF
C7T7	STUFF	STUFF
R5F5	STUFF	STUFF
R5T6	STUFF	STUFF
R5T7	STUFF	STUFF
R5U1	NO-STUFF	STUFF
R5U6	STUFF	STUFF
R6F5	STUFF	STUFF
R6R1	STUFF	STUFF
R6R2	STUFF	STUFF
R6T7	STUFF	STUFF
R6T8	STUFF	STUFF
R6T9	STUFF	STUFF
R6U1	NO-STUFF	STUFF
R7E1	STUFF	STUFF
R7E8	STUFF	STUFF
R7T1	NO-STUFF	STUFF
R7T6	NO-STUFF	STUFF
U5F1	STUFF	STUFF
U5U1	NO-STUFF	STUFF
U5U2	NO-STUFF	STUFF
U6F1	STUFF	STUFF
U6U1	NO-STUFF	STUFF
U7D1	STUFF	STUFF
U7E1	STUFF	STUFF
U7T1	NO-STUFF	STUFF
U7T1	NO-STUFF	STUFF

SROM MEMORY REFDES TO STUFF

REFDES	DEBUG	CPU DBG	XDK	RETAIL
C4R4	STUFF	STUFF	STUFF	NO-STUFF
R4R7	STUFF	STUFF	STUFF	NO-STUFF
R4R9	STUFF	STUFF	STUFF	NO-STUFF
R4R10	NO-STUFF	NO-STUFF	NO-STUFF	NO-STUFF
R4R11	STUFF	STUFF	STUFF	NO-STUFF
R4R12	STUFF	STUFF	STUFF	NO-STUFF

[PAGE_TITLE=COMPONENT STUFFING TABLES]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 71/74	CSA PAGE 71/74	FAB C	REV 1.0

I2C REFERENCE TABLES

DIGITAL POTENTIOMETERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESS
VMEM	256	0.007031V	W: 01011000 0X58, R: 01011001 0X59
VEDRAM	256	0.004199V	W: 01011000 0X58, R: 01011001 0X59
V5P0	256	0.011719V	W: 01011010 0X5A, R: 01011011 0X5B
V3P3	256	0.008V	W: 01011010 0X5A, R: 01011011 0X5B
VREF	256	0.007031V	W: 01011110 0X5E, R: 01011111 0X5F
VCS	256	?V	W: 01011110 0X5E, R: 01011111 0X5F
GPUPCIE	256	0.005859V	W: 01011100 0X5C, R: 01011101 0X5D
CPUPLL_1P8	256	0.007148V	W: 01011100 0X5C, R: 01011101 0X5D
V1P2STBY	?	?V	W: 01010100 0X54, R: 01010101 0X55
V3P3STBY	?	?V	W: 01010100 0X54, R: 01010101 0X55
V1P2	?	?V	W: 01010110 0X56, R: 01010111 0X57

STEPS/STEPSIZE TB UPDATED

ANALOG TO DIGITAL CONVERTERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESS
VMEM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
VEDRAM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
V5P0	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
V3P3	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
VCS	4096	0.000806V	W: 01001000 0X48, R: 01001001 0X49
MEM_VREF	4096	0.000806V	W: 01000110 0X46, R: 01000111 0X47
GPUPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
CPUPLL_1P8	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
V12P0	?	?V	W: 10000000 0X80, R: 10000001 0X81
TEMP SENSOR	?	?V	W: 10011100 0X9C, R: 10011101 0X9D
V5P0STBY	?	?V	W: 10011000 0X98, R: 10011001 0X99
V1P2STBY	?	?V	W: 10000110 0X86, R: 10000111 0X87
V3P3STBY	?	?V	W: 10010010 0X92, R: 10010011 0X93
V1P2	?	?V	W: 10000010 0X82, R: 10000011 0X83

STEPS/STEPSIZE TB UPDATED

WAITSBURG DOC TRACKER

Document#	Document Title
H104359	Waitsburg Document Tree
H101502	Corona Game Console Product Specification
H08676	Console Usage Model And Reliability Budget
H101667	Corona Console Specifications Template
H101671	Corona System Block Diagram
H09424	Vjele Datasheet
H08769	Trinity Console PLL Specification
H101637	Southbridge Security Review
H101786	KSB Programmer's Model
H101787	KSB Register Specification
H101665	Corona Power On Reset Timing Diagram
H08754	Trinity Console Audio / Video Specification
H101664	Corona SMC Firmware Requirements
H102138	Winchester Console Flash Specification
H104793	DataIO Flash Programming Job Creation for Waitsburg eMMC
H104815	Waitsburg Console USB Specification
H08770	Trinity Console Tilt Switch Specification
H09297	Spec,System Fan,High Speed PWM
H09169	Specification,RJ45+Auxiliary Power Connector
H08776	Trinity Console FPM Requirements Document
H08775	Trinity Console FPM LED Display Spec
H09443	Boron Front Panel Module Product Specification
H100727	Trinity Front Panel Module SMC Serial Protocol Specification
H101005	Wave Module Specification
H09553	802.11n Wi-Fi Module Supplier Qualification Requirements
H08757	Trinity Console IR Specification
H02235	Spec,Xenon,Optical Disc Drive Anti Piracy Specification
H08938	Xbox360 Optical Disc Drive Component Specification,Mustang
H08939	Xbox360 Optical Disc Drive Interface Specification,Mustang
H08753	Hard Drive Component Specification
H101663	Corona System Power Budget
H101672	Corona 1/2w Standby Power Budget
H101662	Corona Console VR Architecture
H101572	Spec,ACPT,Sys PS,120w,Small Form Factor;2-Outp W/Fan,1/2w
H08945	Spec,DC Output Cord Assy Acceptance Specification,Dual Barrel
?H08758	Trinity Console V_CPUCORE Regulator Specification (Obsolete?)
H08762	Trinity Console V_5P0 Regulator Specification
H08763	Trinity Console V_3P3 Regulator Specification
H08765	Trinity Console V_EDRAM Regulator Specification
H08764	Trinity Console V_MEM Regulator Specification
H08759	Trinity Console V_CPUVCS Regulator Specification
H101661	Corona Console Linear Regulators Specification
H101659	Corona Console V_3P3STBY Regulator Specification
H101660	Corona Console V_1P2STBY Regulator Specification
H05204	Spec,Xenon PCB Specification,TG150
H07678	Specification Odin Mechanical Design

[PAGE_TITLE=DOC TRACKER]

Change list

- started from Corona Fab E

Sep 26, 2011
- retail:p3, removed CPU_DBGx_POSTx connections to FTPs
- all:p22, modified R3R5 because of updated .ptf entry (was X814857-001, is X814857-001) (was 84.52 KOHM, is 84.5 KOHM)
- all:p30, modified FB2R1 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)
- all:p31, modified FB3P2 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)
- all:p31, modified FB3P1 because of updated .ptf entry (was X857387-001, is X857387-001) (was 0.45 OHM, is 0.45DCR)
- all:p35, modified SW5G2 because of updated .ptf entry (was X800550-004, is X800550-004) (was SM, is TH)
- all:p35, modified SW3G1 because of updated .ptf entry (was X850477-001, is X850477-001) (was _, is SPST)
- all:p38, modified FB2M1 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)
- all:p39, modified FB1A1 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)

Oct 11,2011
- all:p26, added series term to FLSH_DATA<0:7>,FLSH_WP_N,FLSH_CLE,FLSH_CE_N
- all:p26, replaced stitching caps to 25v
- all:p32, removed Phison,NAND, added eMMC
- all:p34, connected NAND after the series term
- all:p33, replaced WM1824 with WM1824B
- all:p44, replaced NCP4201 with NCP4202
- all:p39, combined V_GAMEPORT2 with V_GAMEPORT1,replaced thermistor with X800753-001,removed V_GAMEPORT2 thermistor
- all:p39, combined V_EXPPORT2 with V_EXPPORT1, replaced thermistor with X800753-001, removed V_EXPPORT2 thermistor
- all:p39, updated usbtriple connector symbol

Oct 21, 2011
- xdk:p1, title page
- retail:p1, title page
- xdk:p2, MATERIAL=EMPTY:R4P5,R4P4, BOM=DEVKIT:R4R20, BOM=GCPU_VEJLE_BASE:U5E1
- all:p4, BOM=GDDR_BOTTOM:U5U2,R6U6
- all:p5, BOM=DEVKIT: all parts this page
- all:p9: removed BOM=CORE: all parts this page
- all:p10: removed BOM=CORE: all parts this page
- all:p11: removed BOM=CORE: all parts this page
- all:p14: MATERIAL=EMPTY: U7E1, added PART_LINE_ITEMs for U7E1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7T4, added PART_LINE_ITEM for R7T4
- all:p15: MATERIAL=EMPTY: U7T1, added PART_LINE_ITEMs for U7T1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7E7, added PART_LINE_ITEM for R7E7, BOM=GDDR_BOTTOM:R7T6
- all:p16: MATERIAL=EMPTY: U7D1, added PART_LINE_ITEMs for U7D1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7R4, added PART_LINE_ITEM for R7R4
- all:p17: MATERIAL=EMPTY: U7R1, added PART_LINE_ITEMs for U7R1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7D5, added PART_LINE_ITEM for R7D5, BOM=GDDR_BOTTOM:R7T1
- all:p18: MATERIAL=EMPTY: U5F1, added PART_LINE_ITEMs for U5F1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R5U4, added PART_LINE_ITEM for R5U4
- all:p19: MATERIAL=EMPTY: U5U1, added PART_LINE_ITEMs for U5U1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R5F2, added PART_LINE_ITEM for R5F2, BOM=GDDR_BOTTOM:R5U1
- all:p20: MATERIAL=EMPTY: U6F1, added PART_LINE_ITEMs for U6F1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R6U4, added PART_LINE_ITEM for R6U4
- all:p21: MATERIAL=EMPTY: U6U1, added PART_LINE_ITEMs for U6U1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R6F2, added PART_LINE_ITEM for R6F2, BOM=GDDR_BOTTOM:R6U1
- all:p24: BOM=RETAIL:R2C12, BOM=DEVKIT:R2C11
- all:p25: BOM=RETAIL:R2G4, BOM=DEVKIT:R2G3, BOM=JTM_INT:R3R12, BOM=JTM_EXT:R3R10
- all:p35: BOM=DEVKIT:SW3G1
- xdk:p38: BOM=DEVKIT:R7A1,R7A2,R6B1
- all:p45: X857866-001:Q6B2,Q6B1, X857867-001:Q6C2,Q6C1,Q5C3,Q5C1
- all:p47: X857866-001:Q2F1, X857867-001:Q2F2, BOM=DEVKIT:R2G1, BOM=VREG_FIXED:R2E4,R2T4, X821117-001:R2E5, X801000-001:R2F1
- all:p48: BOM=DEVKIT:R1F19, BOM=VREG_FIXED:R1E20, BOM=VREG_FIXED:R1E19
- all:p49: X857866-001:Q3F1, X857867-001:Q4F1, BOM=DEVKIT:R4F1, BOM=VREG_FIXED:R3F8,R3F9, Part# change:C3F3,C3F2,R3F6,R3F10,R3F7,R3V1
- all:p50: X857866-001:Q7G1, X857867-001:Q7G2, BOM=DEVKIT:R7F1, BOM=VREG_FIXED:R3G11,R3G12, Part# change:C3G7,C3G6,R3V4,R3G13,R3G10,R4G3
- all:p51: X857866-001:Q5B1, X857867-001:Q5C2, BOM=DEVKIT:R5C2, BOM=VREG_FIXED:R4B17,R4B19
- all:p52: BOM=RETAIL:R4B14, added PART_LINE_ITEM for R4B14, BOM=VREG_FIXED:R4B9,R4B7,R4E8,R4E6
- all:p53: BOM=DEVKIT:R4B7,R5A11, BOM=VREG_FIXED:R5B5,C5B1,R5A15,R5A6,C5A1,R5A5, added PART_LINE_ITEMs, BOM=VREG_MM:R5B2,R5A13,R5A8,R5A12
- all:p54: MATERIAL=EMPTY:C7M1,C4N8,C2V2,C3E2,C3C7,C1U3,C4N2
- all:p55: BOM=DEVKIT:R3B1,R3B2,J5B1, BOM=RETAIL:R3C2,R3C1, BOM=VREG_MM: various parts
- all:p56: BOM=VREG_MM: various parts
- all:p57: BOM=VREG_MM: various parts
- all:p58: BOM=VREG_MM: various parts
- all:p59: BOM=VREG_MM: various parts
- all:p60: BOM=VREG_MM: various parts
- all:p61: BOM=JTM_INT: various parts, BOM=JTM_EXT: various parts
- all:p62: BOM=DEVKIT: all parts this page
- all:p65: BOM=DEVKIT: various parts
- all:p67: MATERIAL=EMPTY:LB2B1, added PART_LINE_ITEM for LB2B1
- all:p73: updated to Waitsburg Document tree
- all:p74: this page

Dec 26, 2011
- all:p32: changed R1D4 from X801814-001 to X806693-001
- all:p53: changed R5A4 from NO-STUFF to STUFF, changed R5A7,C5M8,C5M5 to NO-STUFF

Schematic Transitions for Waitsburg

This document lists the schematic changes needed to transform Waitsburg Fab A from Debug to XDK to Retail.
The base schematic is Waitsburg Fab A Debug

Waitsburg Debug to XDK changes
Start from Waitsburg Fab A Debug and replace the following files/pages:
page1.csa: Rename title page to XDK
page12.csa: Delete nets MA_A<12>, MB_A<12>
page13.csa: Delete nets MC_A<12>, MD_A<12>
page14.csa: Delete nets MA_A<12>, stuff R7T5,R7T4 (MEM_A_VREF1 resistor divider)
page15.csa: Delete nets MA_A<12>, stuff R7E6,R7E7 (MEM_A_VREF0 resistor divider)
page16.csa: Delete nets MB_A<12>, stuff R7R2,R7R4 (MEM_B_VREF1 resistor divider)
page17.csa: Delete nets MB_A<12>, stuff R7D4,R7D5 (MEM_B_VREF0 resistor divider)
page18.csa: Delete nets MC_A<12>, stuff R5U5,R5U4 (MEM_C_VREF1 resistor divider)
page19.csa: Delete nets MC_A<12>, stuff R5F1,R5F2 (MEM_C_VREF0 resistor divider)
page20.csa: Delete nets MD_A<12>, stuff R6U5,R6U4 (MEM_D_VREF1 resistor divider)
page21.csa: Delete nets MD_A<12>, stuff R6F1,R6F2 (MEM_D_VREF0 resistor divider)
page62.csa: Delete MEM_VREFS shunt circuitry
page63.csa: blank, deleted entire page
page64.csa: blank, deleted entire page

Waitsburg XDK to Retail changes
Start from Waitsburg Fab A XDK and replace the following files/pages:
page1.csa: Rename title page to RETAIL
page2.csa: Delete CPU_TE pulldown resistor (R4R20) and tie U5E1.E7 to ground
page3.csa: Disconnect U5E1 TB[0:7],TB[11:15] from CPU_DBG<0..15> bus, ground FTPs for TB[0:7], float FTPs for TB[11:15]
page5.csa: Diconnect U5E1.E3 (SROM_EN) from pullup resistor (R4R2)
page25.csa: Short U3D1.A6 (SMC_UART1_RXD) to V_3P3STBY
page38.csa: Delete V_12P0 shunt resistors (R7A1,R7A2), short V_12P0 to J7A1 pins 5-8. Remove short_parts (ST7A1,ST7A2).
page38.csa: Delete V_5P0STBY shunt resistor (R6B1), short V_5P0STBY to J7A1.10. Remove short_parts (ST6B1,ST6B2)
page47.csa: Delete V_5P0 shunt resistor (R2G1), short V_5P0 to L2F1.2. Remove short_parts (ST2G2,ST2G3)
page48.csa: Delete V_3P3 shunt resistor (R1F9), short V_3P3 to L1F1.2. Remove short_parts (ST1F1,ST1F3)
page49.csa: Delete V_CPUEDRAM shunt resistor (R4F1), short V_CPUEDRAM to L4F1.2. Remove short_parts (ST4F2,ST4F4)
page50.csa: Delete V_MEM shunt resistor (R7F1), short V_MEM to L7F1.1. Remove short_parts (ST7F2,ST7F3)
page51.csa: Delete V_CPUVCS shunt resistor (R5C2), short V_CPUVCS to L5C1.2. Remove short_parts (ST5C1,ST5C3)
page52.csa: Delete V_5P0 shunt resistor (R2G1), short V_5P0 to L2F1.2. Remove short_parts (ST2G2,ST2G3)
page53.csa: Delete V_1P2 shunt resistor (R4B14), short V_1P2 to U3B1.4. Remove short_parts (ST4B1,ST4B2). Remove PART_LINE_ITEM FOR R4B14
page53.csa: Delete V_GPUPCIE shunt resistor (R4E11), short V_GPUPCIE to U4E2 pin 2 and 4.
page53.csa: Delete V_1P8 shunt resistor (R4E12), short V_1P8 to U4E1.2. Delete V_CPUPLL shunt resistor (R4E4) replace with short_part
page53.csa: Delete V_EFUSE shunt resistor (R4P10), short V_EFUSE to U4P2.5.
page62.csa: Delete PCIe mid-bus probe (J3E1). Delete GPU_CLK probe (J4D2). Delete SMC_DBG_RXD filter (R2C2,C2C1). Float J2C3.3
page65.csa: Delete DBPADs to V_5P0, V_3P3, GND

Caveat:
On the Waitsburg Debug, page 38, there is a thermistor, RT3B1. This thermistor is the same thermistor on Waitsburg Retail, page 38, RT3A2.
During layout, ref des were renumbered on the Waitsburg Retail schematic page.
TO DO: Respin Waitsburg Retail schematic and fab and change RT3A2 to RT3B1
TO DO: Respin Waitsburg Retail schematic and fab and change RT3A2 to RT3B1
TO DO: Respin Waitsburg Retail schematic and fab and change RT3A2 to RT3B1

MICROSOFT CONFIDENTIAL	PROJECT NAME STINGRAY	PAGE 74/74	CSA PAGE 74/74	FAB C	REV 1.0