WAITSBURG REV 1.0 FAB B RETAIL

Rules: (when possible)
* MSB-->LSB: top-->bottom
* When possible: inputs on left, outputs on right
* Page order: chip interfaces, termination, power, decoupling
* Avoid off-page connectors for on-page connections
* Bussed signals are grouped on symbols
* Unnamed nets are displayed with half-sized text
* Transmitter name used as prefix with RX and TX connections
* V_ prefix for voltage rail signal names
* _DP/_DN suffix for differential pairs
* _N suffix for active low or n junction
* _P suffix for p junction
* _EN suffix for enable
* CLK for clock, RST for reset
* PWRGD for power good
* Rev and fab set with custom variables. Tools->options->variables

[PAGE_TITLE=COVER PAGE]

DRAWING Wed Mar 14 01:45:02 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	1/74	B	1.0

GCPU SETUP

25 IN CPU_RST_N — FT3T10 FTP 1

R4P5 2 1 1.27 KOHM 1% 402 EMPTY

1 C5R11 360 PF 5% 50 V 2 EMPTY 603

1 R4P4 2 KOHM 1% 2 EMPTY 402

CPU_RST_V1P1_N OUT 65

FT3T11 FTP 1

65 25 IN CPU_PWRGD

1 R3E10 10 KOHM 5% 2 CH 402

1 C5R66 360 PF 5% 50 V 2 EMPTY 603

GCPU_VEJLE_BASE

U5E1 14 OF 17 IC

GCPU VERSION 1

D5 HARD_RESET_B

T5 POWER_GOOD

CHECKSTOP_B E5 — CPU_CHECKSTOP_N OUT 65

22 IN CPU_CLK_DP — R4D1 2 1 0 OHM 5% 402 CH

IN CPU_CLK_DP_R2 — P2 CPU_CLK_DP

22 IN CPU_CLK_DN — R4D2 2 1 0 OHM 5% 402 CH

IN CPU_CLK_DN_R2 — P1 CPU_CLK_DN

V_CPUCORE

I112

1 R4R22 100 OHM 5% 2 EMPTY 402

1 R4R23 100 OHM 5% 2 EMPTY 402

CPU_DBG_RST_EN	INTERNAL PULLDN
GPU_DBG_RST_EN	INTERNAL PULLDN

DB4R3 1 1 DB4R2

CPU_DBG_RST_EN — P5 CPU_DBG_RST_EN<DN>

GPU_DBG_RST_EN — R5 GPU_DBG_RST_EN<DN>

VID6 C24 — CPU_VREG_APS6 OUT 43

VID5 B24 — CPU_VREG_APS5 OUT 43

VID4 A24 — CPU_VREG_APS4 OUT 43

VID3 C23 — CPU_VREG_APS3 OUT 43

VID2 B23 — CPU_VREG_APS2 OUT 43

VID1 A23 — CPU_VREG_APS1 OUT 43

1 1 FTP FT7P8

1 1 FTP FT7P7

1 1 FTP FT7P6

1 1 FTP FT7P5

1 1 FTP FT7P4

1 1 FTP FT7P3

OUT EDRAM_PSRO_DOUT — N6 PSRO_DOUT

OUT CPU_PSRO0_OUT — G7 PSRO0_OUT

V_CPUPLL

WHEN V_CPUPLL=1.83V
SET VGATE=1.20V
ACTUAL=1.202V

N: IF V_CPUPLL CHANGES
VGATE RESISTORS SHOULD BE ADJUSTED

1 R5T8 562 OHM 1% 2 CH 402

CPU_VGATE — V6 V_GATE

1 R5T9 1.07 KOHM 1% 2 CH 402

<DN>PULSE_LIMIT_BYPASS

<DN>PLL_BYPASS

J6 — CPU_LIMIT_BYPASS OUT

F8 — CPU_PLL_BYPASS OUT

OUT RESISTOR0_DP — L7 RESISTOR0_DP

OUT RESISTOR0_DN — M7 RESISTOR0_DN

SRVID A3 — CPU_SRVID OUT 51

EFU_POWERON C1 — VREG_EFUSE_EN OUT 52

OUT CPU_EXT_CLK_EN — F7 EXT_CLK_EN<DN>

CPU_TINIT — J7 TI_39_TINIT

CPU_TE — E7 TE

CORE_HF_BGR_PLL M6 — CORE_HF_BGR_PLL OUT

1 R4R21 200 OHM 5% 2 CH 402

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6 LAYER ONLY SIGNALS

CORE_HF_BGR_PLL	6 LAYER ONLY; TP ONLY
CPU_LIMIT_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_PLL_BYPASS	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_CORE_HF_CLKOUT_DN	6 LAYER ONLY; TP ONLY
CPU_CORE_HF_CLKOUT_DP	6 LAYER ONLY; TP ONLY
CPU_EXT_CLK_EN	6 LAYER ONLY; TP ONLY, INTERNAL PULLDN
CPU_DLL_SNIF_OUT	6 LAYER ONLY; TP ONLY
CPU_VDDS0_DP	6 LAYER ONLY
CPU_VDDS0_DN	6 LAYER ONLY
CPU_VDDS1_DP	6 LAYER ONLY
CPU_VDDS1_DN	6 LAYER ONLY
RESISTOR0_DP	6 LAYER ONLY
RESISTOR0_DN	6 LAYER ONLY
EDRAM_PSRO_DOUT	6 LAYER ONLY

[PAGE_TITLE=GCPU SETUP]

DRAWING
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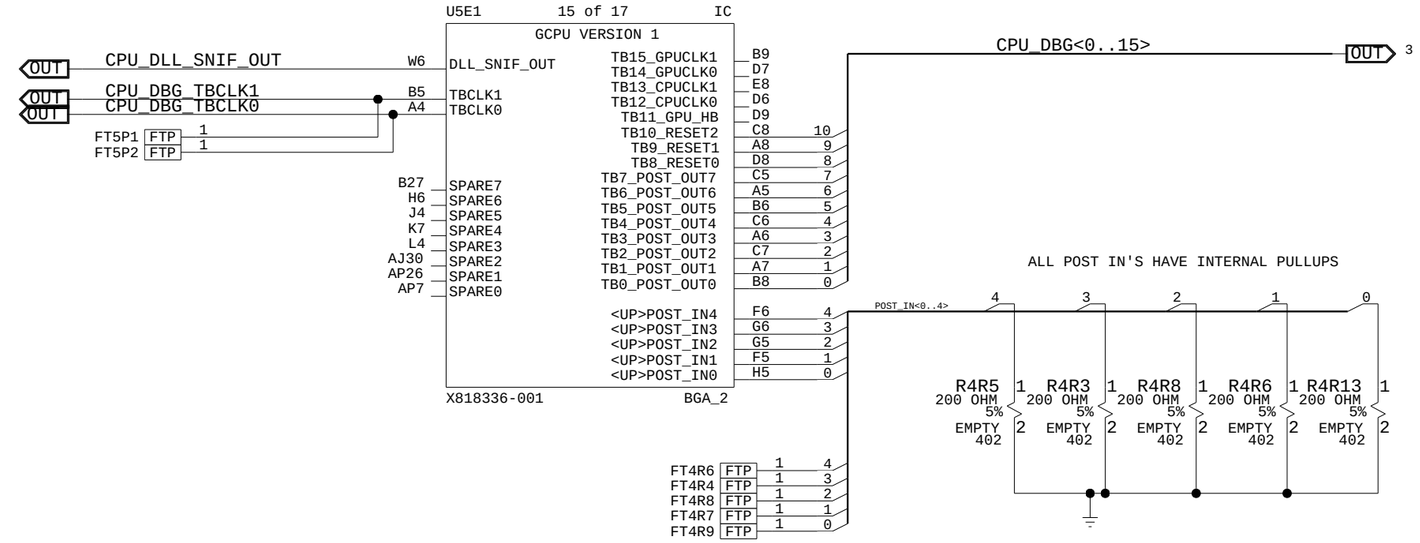
MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 2/74	FAB B	REV 1.0

GCPU, DEBUG BUS



[PAGE_TITLE=GCPU, DEBUG BUS]

DRAWING
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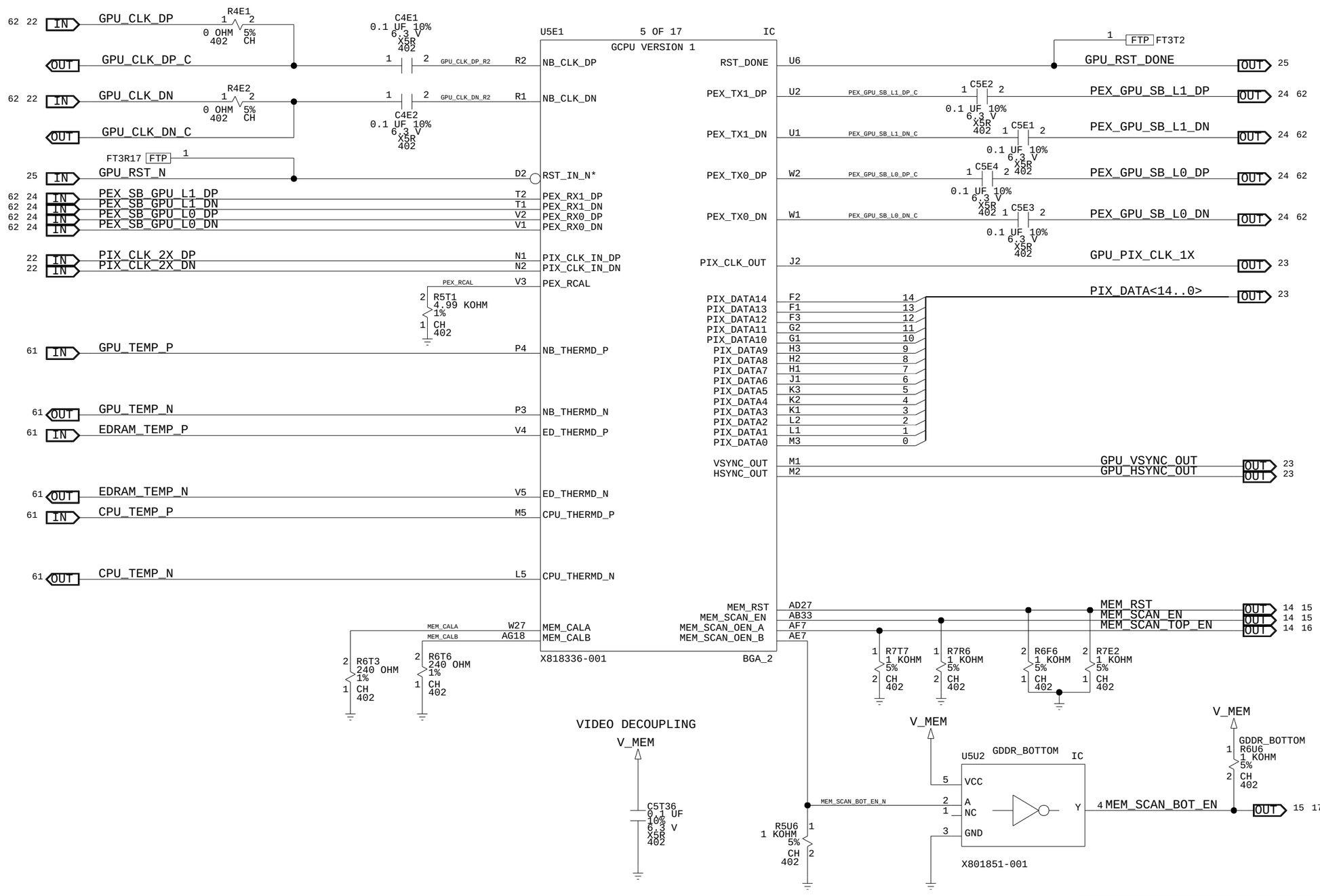
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	3/74	B	1.0

GCPU, VIDEO + PCIEX



[PAGE_TITLE=GCPU, VIDEO + PCIEX]

DRAWING
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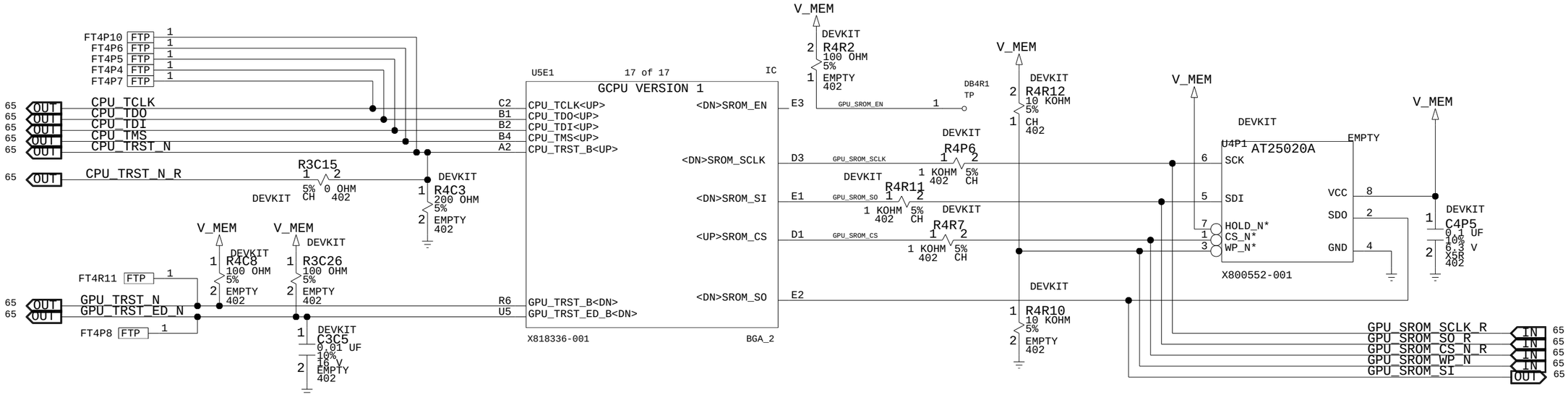
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	4/74	B	1.0

GCPU, EEPROM + JTAG



[PAGE_TITLE=GCPU, EEPROM + JTAG]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	5/74	B	1.0

GCPU, PLL POWER + FSB POWER

V_GPUPCIE V_CPUEDRAM V_CPUPLL V_EFUSE

U5E1 16 of 17 IC

GCPU VERSION 1

OUT CPU_VDDS1_DP
OUT CPU_VDDS1_DN
OUT CPU_VDDS0_DP
OUT CPU_VDDS0_DN

E4 VDDE
H25 VDDS1_DP
J26 VDDS1_DN
P7 VDDS0_DP
N7 VDDS0_DN

CORE_HF_CLKOUT_DP L6 OUT CPU_CORE_HF_CLKOUT_DP
CORE_HF_CLKOUT_DN K6 OUT CPU_CORE_HF_CLKOUT_DN

FB5R1 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5R14 10 UF 20% 6.3 V X5R 805 — ST5R1 SHORT
V_CPU_PVDDA_MEM → D4 PVDDA_MEM
V_CPU_PVSSA_MEM → C4 PVSSA_MEM

FB5T2 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5T9 10 UF 20% 6.3 V X5R 805 — ST5T1 SHORT
V_CPU_PVDDA_PEX → U3 PVDDA_PEX
V_CPU_PVSSA_PEX → U4 PVSSA_PEX

FB5R2 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5R17 10 UF 20% 6.3 V X5R 805 — ST5R2 SHORT
V_CPU_PVDDA_HS → C3 PVDDA_HS
V_CPU_PVSSA_HS → B3 PVSSA_HS

FB5T3 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5T13 4.7 UF 10% 6.3 V X5R 603 — ST5T2 SHORT
V_CPU_PVDDA_ED → W5 PVDDA_ED
V_CPU_PVSSA_ED → W4 PVSSA_ED

DB5R5

FB5R5 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5R54 10 UF 20% 6.3 V X5R 805 — ST5R5 SHORT
V_CPU_VDDA_RNG → N4 VDDA_RNG
V_CPU_GNDA_RNG → N3 GNDA_RNG

FB5R4 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5R42 10 UF 20% 6.3 V X5R 805 — ST5R4 SHORT
V_CPU_CORE_HF_VDDA_PLL → J5 CORE_HF_VDDA_PLL
V_CPU_CORE_HF_GNDA_PLL → K5 CORE_HF_GNDA_PLL

FB5R3 — 120 OHM 0.2A A 0.5DCR — FB 603 — C5R31 10 UF 20% 6.3 V X5R 805 — ST5R3 SHORT
V_GPU_VDDA_PLL → G4 GPU_VDDA_PLL
V_GPU_GNDA_PLL → H4 GPU_GNDA_PLL

R3 VDD_VTT

FB5T1 — 120 OHM 0.2A A 0.5DCR — FB 603
V_CPU_VDD_VTTA → R4 VDD_VTTA

C5T4 4.7 UF 10% 6.3 V X5R 603
C5T6 0.1 UF 10% 6.3 V X5R 402

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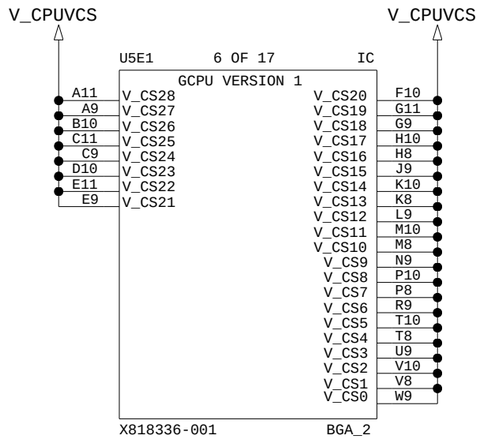
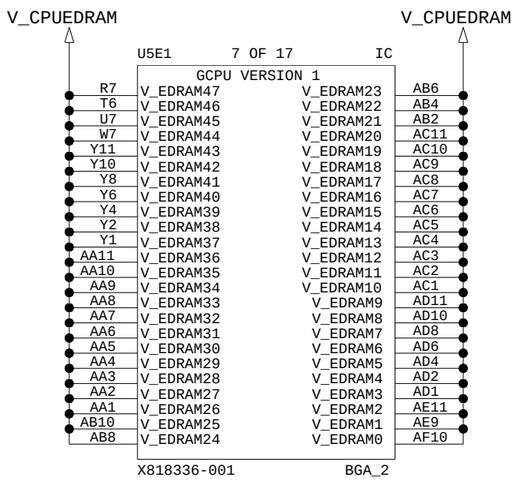
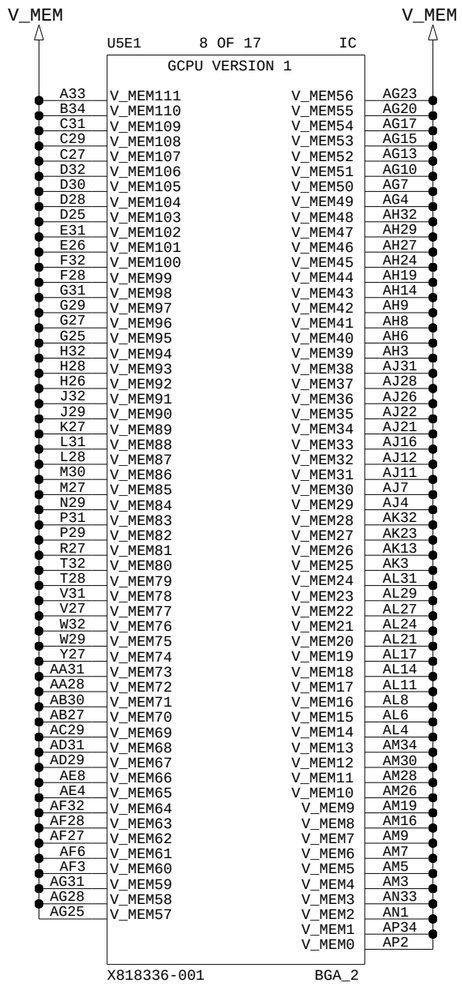
[PAGE_TITLE=GCPU, PLL POWER + FSB POWER]

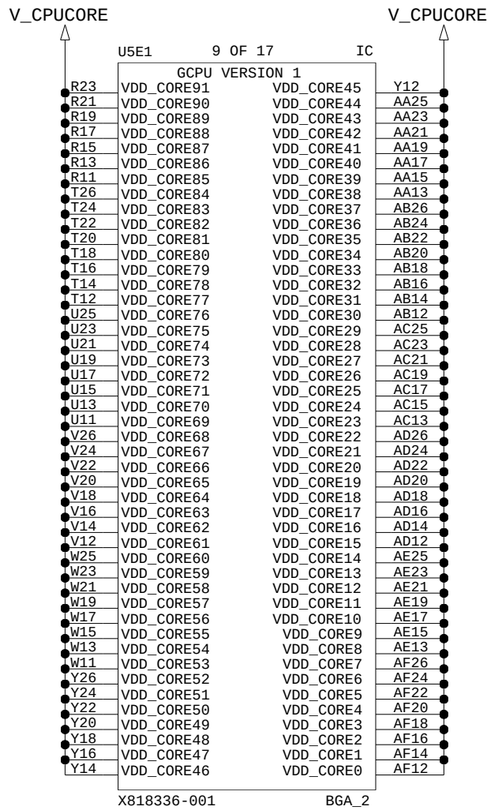
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	6/74	B	1.0

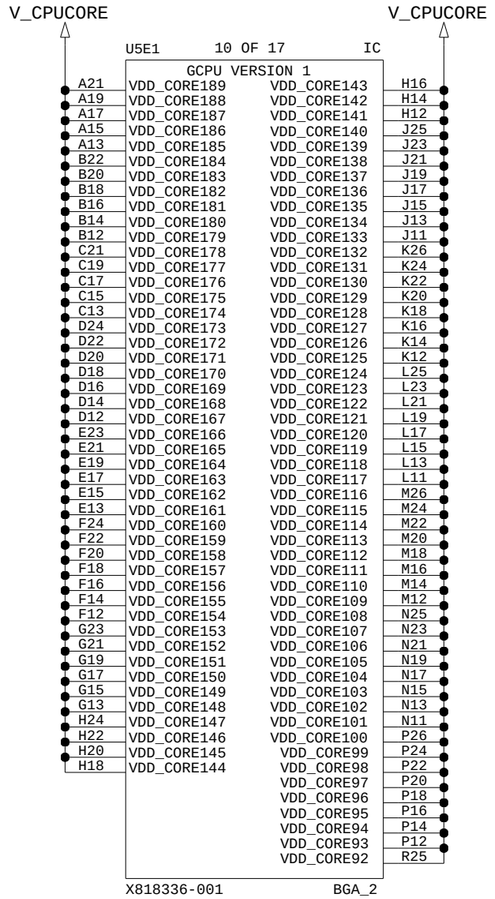
GCPU, POWER











[PAGE_TITLE=GCPU, POWER]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	7/74	B	1.0

GCPU, POWER

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GCPU VERSION 1

Y3	VSS130	VSS65	AF15
AA32	VSS129	VSS64	AF13
AA27	VSS128	VSS63	AF11
AA26	VSS127	VSS62	AF9
AA24	VSS126	VSS61	AF8
AA22	VSS125	VSS60	AF4
AA20	VSS124	VSS59	AG32
AA18	VSS123	VSS58	AG29
AA16	VSS122	VSS57	AG27
AA14	VSS121	VSS56	AG26
AA12	VSS120	VSS55	AG24
AB25	VSS119	VSS54	AG22
AB23	VSS118	VSS53	AG21
AB21	VSS117	VSS52	AG19
AB19	VSS116	VSS51	AG16
AB17	VSS115	VSS50	AG14
AB15	VSS114	VSS49	AG12
AB13	VSS113	VSS48	AG11
AB11	VSS112	VSS47	AG9
AB9	VSS111	VSS46	AG8
AB7	VSS110	VSS45	AG6
AB5	VSS109	VSS44	AG3
AB3	VSS108	VSS43	AH31
AB1	VSS107	VSS42	AH28
AC31	VSS106	VSS41	AH7
AC27	VSS105	VSS40	AH4
AC26	VSS104	VSS39	AJ32
AC24	VSS103	VSS38	AJ29
AC22	VSS102	VSS37	AJ27
AC20	VSS101	VSS36	AJ25
AC18	VSS100	VSS35	AJ20
AC16	VSS99	VSS34	AJ17
AC14	VSS98	VSS33	AJ15
AC12	VSS97	VSS32	AJ10
AD32	VSS96	VSS31	AJ8
AD25	VSS95	VSS30	AJ6
AD23	VSS94	VSS29	AJ3
AD21	VSS93	VSS28	AK31
AD19	VSS92	VSS27	AK18
AD17	VSS91	VSS26	AK4
AD15	VSS90	VSS25	AL32
AD13	VSS89	VSS24	AL30
AD9	VSS88	VSS23	AL28
AD7	VSS87	VSS22	AL26
AD5	VSS86	VSS21	AL22
AD3	VSS85	VSS20	AL19
AE29	VSS84	VSS19	AL16
AE27	VSS83	VSS18	AL12
AE26	VSS82	VSS17	AL9
AE24	VSS81	VSS16	AL7
AE22	VSS80	VSS15	AL5
AE20	VSS79	VSS14	AL3
AE18	VSS78	VSS13	AM33
AE16	VSS77	VSS12	AM31
AE14	VSS76	VSS11	AM29
AE12	VSS75	VSS10	AM27
AE10	VSS74	VSS9	AM24
AE6	VSS73	VSS8	AM21
AE3	VSS72	VSS7	AM14
AF31	VSS71	VSS6	AM11
AF25	VSS70	VSS5	AM8
AF23	VSS69	VSS4	AM6
AF21	VSS68	VSS3	AM4
AF19	VSS67	VSS2	AN34
AF17	VSS66	VSS1	AP33
		VSS0	AP1

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U5E1 12 OF 17 IC

GCPU VERSION 1

K29	VSS260	VSS195	R16
K25	VSS259	VSS194	R14
K23	VSS258	VSS193	R12
K21	VSS257	VSS192	R10
K19	VSS256	VSS191	R8
K17	VSS255	VSS190	T31
K15	VSS254	VSS189	T27
K13	VSS253	VSS188	T25
K11	VSS252	VSS187	T23
K9	VSS251	VSS186	T21
K4	VSS250	VSS185	T19
L32	VSS249	VSS184	T17
L27	VSS248	VSS183	T15
L26	VSS247	VSS182	T13
L24	VSS246	VSS181	T11
L22	VSS245	VSS180	T9
L20	VSS244	VSS179	T7
L18	VSS243	VSS178	T4
L16	VSS242	VSS177	T3
L14	VSS241	VSS176	U30
L12	VSS240	VSS175	U27
L10	VSS239	VSS174	U26
L8	VSS238	VSS173	U24
L3	VSS237	VSS172	U22
M25	VSS236	VSS171	U20
M23	VSS235	VSS170	U18
M21	VSS234	VSS169	U16
M19	VSS233	VSS168	U14
M17	VSS232	VSS167	U12
M15	VSS231	VSS166	U10
M13	VSS230	VSS165	U8
M11	VSS229	VSS164	V29
M9	VSS228	VSS163	V25
M4	VSS227	VSS162	V23
N31	VSS226	VSS161	V21
N27	VSS225	VSS160	V19
N26	VSS224	VSS159	V17
N24	VSS223	VSS158	V15
N22	VSS222	VSS157	V13
N20	VSS221	VSS156	V11
N18	VSS220	VSS155	V9
N16	VSS219	VSS154	V7
N14	VSS218	VSS153	W31
N12	VSS217	VSS152	W26
N10	VSS216	VSS151	W24
N8	VSS215	VSS150	W22
N5	VSS214	VSS149	W20
P32	VSS213	VSS148	W18
P27	VSS212	VSS147	W16
P25	VSS211	VSS146	W14
P23	VSS210	VSS145	W12
P21	VSS209	VSS144	W10
P19	VSS208	VSS143	W8
P17	VSS207	VSS142	W3
P15	VSS206	VSS141	Y29
P13	VSS205	VSS140	Y25
P11	VSS204	VSS139	Y23
P9	VSS203	VSS138	Y21
P6	VSS202	VSS137	Y19
R29	VSS201	VSS136	Y17
R26	VSS200	VSS135	Y15
R24	VSS199	VSS134	Y13
R22	VSS198	VSS133	Y9
R20	VSS197	VSS132	Y7
R18	VSS196	VSS131	Y5

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U5E1 13 OF 17 IC

GCPU VERSION 1

A34	VSS354	VSS318	E24
A22	VSS353	VSS317	E22
A20	VSS352	VSS316	E20
A18	VSS351	VSS315	E18
A16	VSS350	VSS314	E16
A14	VSS349	VSS313	E14
A12	VSS348	VSS312	E12
A10	VSS347	VSS311	E10
B33	VSS346	VSS310	E6
B21	VSS345	VSS309	F31
B19	VSS344	VSS308	F29
B17	VSS343	VSS307	F27
B15	VSS342	VSS306	F23
B13	VSS341	VSS305	F21
B11	VSS340	VSS304	F19
B7	VSS339	VSS303	F17
C28	VSS338	VSS302	F15
C25	VSS337	VSS301	F13
C22	VSS336	VSS300	F11
C20	VSS335	VSS299	F9
C18	VSS334	VSS298	F4
C16	VSS333	VSS297	G32
C14	VSS332	VSS296	G28
C12	VSS331	VSS295	G24
C10	VSS330	VSS294	G22
D31	VSS329	VSS293	G20
D29	VSS328	VSS292	G18
D27	VSS327	VSS291	G16
D23	VSS326	VSS290	G14
D21	VSS325	VSS289	G12
D19	VSS324	VSS288	G10
D17	VSS323	VSS287	G8
D15	VSS322	VSS286	G3
D13	VSS321	VSS285	H31
D11	VSS320	VSS284	H29
E32	VSS319	VSS283	H27
		VSS282	H23
		VSS281	H21
		VSS280	H19
		VSS279	H17
		VSS278	H15
		VSS277	H13
		VSS276	H11
		VSS275	H9
		VSS274	H7
		VSS273	J31
		VSS272	J27
		VSS271	J24
		VSS270	J22
		VSS269	J20
		VSS268	J18
		VSS267	J16
		VSS266	J14
		VSS265	J12
		VSS264	J10
		VSS263	J8
		VSS261	J3

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[PAGE_TITLE=GCPU, POWER]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	8/74	B	1.0

GCPU, DECOUPLING

V_CPUCORE

C6R4 1 2 4.7 UF 10% 6.3 V X5R 603
C5D13 1 2 4.7 UF 10% 6.3 V X5R 603
C5R8 1 2 4.7 UF 10% 6.3 V X5R 603
C5R9 1 2 4.7 UF 10% 6.3 V X5R 603
C5R15 1 2 4.7 UF 10% 6.3 V X5R 603
C5D14 1 2 4.7 UF 10% 6.3 V X5R 603
C6D3 1 2 4.7 UF 10% 6.3 V X5R 603
C5D7 1 2 4.7 UF 10% 6.3 V X5R 603
C6R3 1 2 4.7 UF 10% 6.3 V X5R 603
C5D3 1 2 4.7 UF 10% 6.3 V X5R 603
C5R7 1 2 4.7 UF 10% 6.3 V X5R 603
C5D6 1 2 4.7 UF 10% 6.3 V X5R 603
C5R10 1 2 4.7 UF 10% 6.3 V X5R 603
C5D8 1 2 4.7 UF 10% 6.3 V X5R 603
C6R6 1 2 4.7 UF 10% 6.3 V X5R 603
C5D5 1 2 4.7 UF 10% 6.3 V X5R 603
C5D12 1 2 4.7 UF 10% 6.3 V X5R 603
C5R6 1 2 4.7 UF 10% 6.3 V X5R 603
C6D4 1 2 4.7 UF 10% 6.3 V X5R 603
C5D9 1 2 4.7 UF 10% 6.3 V X5R 603
C6R2 1 2 4.7 UF 10% 6.3 V X5R 603
C5R5 1 2 4.7 UF 10% 6.3 V X5R 603
C6R1 1 2 4.7 UF 10% 6.3 V X5R 603
C5R18 1 2 4.7 UF 10% 6.3 V X5R 603
C5R12 1 2 4.7 UF 10% 6.3 V X5R 603
C5D2 1 2 4.7 UF 10% 6.3 V X5R 603
C5R3 1 2 4.7 UF 10% 6.3 V X5R 603
C5D10 1 2 4.7 UF 10% 6.3 V X5R 603
C6D5 1 2 4.7 UF 10% 6.3 V X5R 603
C5R16 1 2 4.7 UF 10% 6.3 V X5R 603
C6R7 1 2 4.7 UF 10% 6.3 V X5R 603
C5D11 1 2 4.7 UF 10% 6.3 V X5R 603
C6D1 1 2 4.7 UF 10% 6.3 V X5R 603
C6D2 1 2 4.7 UF 10% 6.3 V X5R 603
C6D6 1 2 4.7 UF 10% 6.3 V X5R 603
C5T33 1 2 4.7 UF 10% 6.3 V X5R 603
C6R5 1 2 4.7 UF 10% 6.3 V X5R 603
C5R13 1 2 4.7 UF 10% 6.3 V X5R 603
C5R2 1 2 4.7 UF 10% 6.3 V X5R 603
C6T22 1 2 4.7 UF 10% 6.3 V X5R 603
C6T23 1 2 4.7 UF 10% 6.3 V X5R 603

V_CPUEDRAM

C5T26 1 2 0.1 UF 10% 6.3 V X5R 402
C5E6 1 2 4.7 UF 10% 6.3 V X5R 603
C5T32 1 2 0.1 UF 10% 6.3 V X5R 402
C5E5 1 2 4.7 UF 10% 6.3 V X5R 603
C5T24 1 2 0.1 UF 10% 6.3 V X5R 402
C5T35 1 2 4.7 UF 10% 6.3 V X5R 603
C5T31 1 2 0.1 UF 10% 6.3 V X5R 402
C5E7 1 2 4.7 UF 10% 6.3 V X5R 603
C5T27 1 2 0.1 UF 10% 6.3 V X5R 402
C5T34 1 2 4.7 UF 10% 6.3 V X5R 603
C5T22 1 2 0.1 UF 10% 6.3 V X5R 402
C5T43 1 2 4.7 UF 10% 6.3 V X5R 603
C5T23 1 2 0.1 UF 10% 6.3 V X5R 402
C5E8 1 2 4.7 UF 10% 6.3 V X5R 603
C5T20 1 2 0.1 UF 10% 6.3 V X5R 402
C5E9 1 2 4.7 UF 10% 6.3 V X5R 603
C5T25 1 2 0.1 UF 10% 6.3 V X5R 402
C4T3 1 2 4.7 UF 10% 6.3 V X5R 603
C5T21 1 2 0.1 UF 10% 6.3 V X5R 402
C4T4 1 2 4.7 UF 10% 6.3 V X5R 603

V_CPUVCS

C5R35 1 2 0.1 UF 10% 6.3 V X5R 402
C5D1 1 2 4.7 UF 10% 6.3 V X5R 603
C5R58 1 2 0.1 UF 10% 6.3 V X5R 402
C5R4 1 2 4.7 UF 10% 6.3 V X5R 603
C5R43 1 2 0.1 UF 10% 6.3 V X5R 402
C5D4 1 2 4.7 UF 10% 6.3 V X5R 603
C5T7 1 2 0.1 UF 10% 6.3 V X5R 402
C5R1 1 2 4.7 UF 10% 6.3 V X5R 603
C5R50 1 2 0.1 UF 10% 6.3 V X5R 402
C5T1 1 2 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 9/74	FAB B	REV 1.0

GCPU, DECOUPLING

V_CPUCORE

C5T12	C5R26	C5T17	C5T10	C6R36
C5R33	C6R25	C6T11	C5T8	C5R63
C5R39	C5R60	C6R42	C6R45	C5R28
C5R40	C5R61	C5R37	C5R49	C5R59
C6T7	C6T20	C6R37	C6R33	C5R27
C5R38	C5R32	C5R57	C6T8	C5R62
C6T12	C6T6	C5R64	C6R15	C5R55
C6R31	C6R28	C5R46	C6R21	C5R51
C6R38	C5R36	C5R45	C6R20	C6R18
C6R43	C5T11	C6T14	C6R44	C6R17

Each: 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	10/74	B	1.0

GCPU, DECOUPLING

V_CPUCORE

C5R25 1 2 0.1 UF 10% 6.3 V X5R 402
C6R8 1 2 0.1 UF 10% 6.3 V X5R 402
C6R39 1 2 0.1 UF 10% 6.3 V X5R 402
C5R30 1 2 0.1 UF 10% 6.3 V X5R 402
C6T5 1 2 0.1 UF 10% 6.3 V X5R 402
C5T14 1 2 0.1 UF 10% 6.3 V X5R 402

C6T15 1 2 0.1 UF 10% 6.3 V X5R 402
C6R34 1 2 0.1 UF 10% 6.3 V X5R 402
C6T3 1 2 0.1 UF 10% 6.3 V X5R 402
C5R52 1 2 0.1 UF 10% 6.3 V X5R 402
C5R21 1 2 0.1 UF 10% 6.3 V X5R 402
C6T9 1 2 0.1 UF 10% 6.3 V X5R 402

C5T19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R35 1 2 0.1 UF 10% 6.3 V X5R 402
C5T15 1 2 0.1 UF 10% 6.3 V X5R 402
C5T16 1 2 0.1 UF 10% 6.3 V X5R 402
C5T3 1 2 0.1 UF 10% 6.3 V X5R 402

C6T18 1 2 0.1 UF 10% 6.3 V X5R 402
C5R53 1 2 0.1 UF 10% 6.3 V X5R 402
C6R22 1 2 0.1 UF 10% 6.3 V X5R 402
C5T28 1 2 0.1 UF 10% 6.3 V X5R 402
C6T19 1 2 0.1 UF 10% 6.3 V X5R 402
C6R13 1 2 0.1 UF 10% 6.3 V X5R 402

C6R9 1 2 0.1 UF 10% 6.3 V X5R 402
C5T30 1 2 0.1 UF 10% 6.3 V X5R 402
C5R44 1 2 0.1 UF 10% 6.3 V X5R 402
C5R41 1 2 0.1 UF 10% 6.3 V X5R 402
C6T25 1 2 0.1 UF 10% 6.3 V X5R 402
C5R34 1 2 0.1 UF 10% 6.3 V X5R 402

C6R10 1 2 0.1 UF 10% 6.3 V X5R 402
C5T29 1 2 0.1 UF 10% 6.3 V X5R 402
C5R47 1 2 0.1 UF 10% 6.3 V X5R 402
C6R24 1 2 0.1 UF 10% 6.3 V X5R 402
C6R12 1 2 0.1 UF 10% 6.3 V X5R 402
C6R14 1 2 0.1 UF 10% 6.3 V X5R 402

C5R20 1 2 0.1 UF 10% 6.3 V X5R 402
C5R24 1 2 0.1 UF 10% 6.3 V X5R 402
C5R48 1 2 0.1 UF 10% 6.3 V X5R 402
C6T2 1 2 0.1 UF 10% 6.3 V X5R 402
C5T2 1 2 0.1 UF 10% 6.3 V X5R 402
C5T5 1 2 0.1 UF 10% 6.3 V X5R 402

C5R19 1 2 0.1 UF 10% 6.3 V X5R 402
C5R56 1 2 0.1 UF 10% 6.3 V X5R 402
C6R26 1 2 0.1 UF 10% 6.3 V X5R 402
C6T16 1 2 0.1 UF 10% 6.3 V X5R 402
C6T17 1 2 0.1 UF 10% 6.3 V X5R 402
C6T13 1 2 0.1 UF 10% 6.3 V X5R 402

C5R22 1 2 0.1 UF 10% 6.3 V X5R 402
C6T4 1 2 0.1 UF 10% 6.3 V X5R 402
C6R32 1 2 0.1 UF 10% 6.3 V X5R 402
C5T18 1 2 0.1 UF 10% 6.3 V X5R 402
C6R40 1 2 0.1 UF 10% 6.3 V X5R 402
C6T24 1 2 0.1 UF 10% 6.3 V X5R 402

C5R23 1 2 0.1 UF 10% 6.3 V X5R 402
C5R29 1 2 0.1 UF 10% 6.3 V X5R 402
C6R29 1 2 0.1 UF 10% 6.3 V X5R 402
C6R30 1 2 0.1 UF 10% 6.3 V X5R 402
C6R41 1 2 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=GCPU, DECOUPLING]

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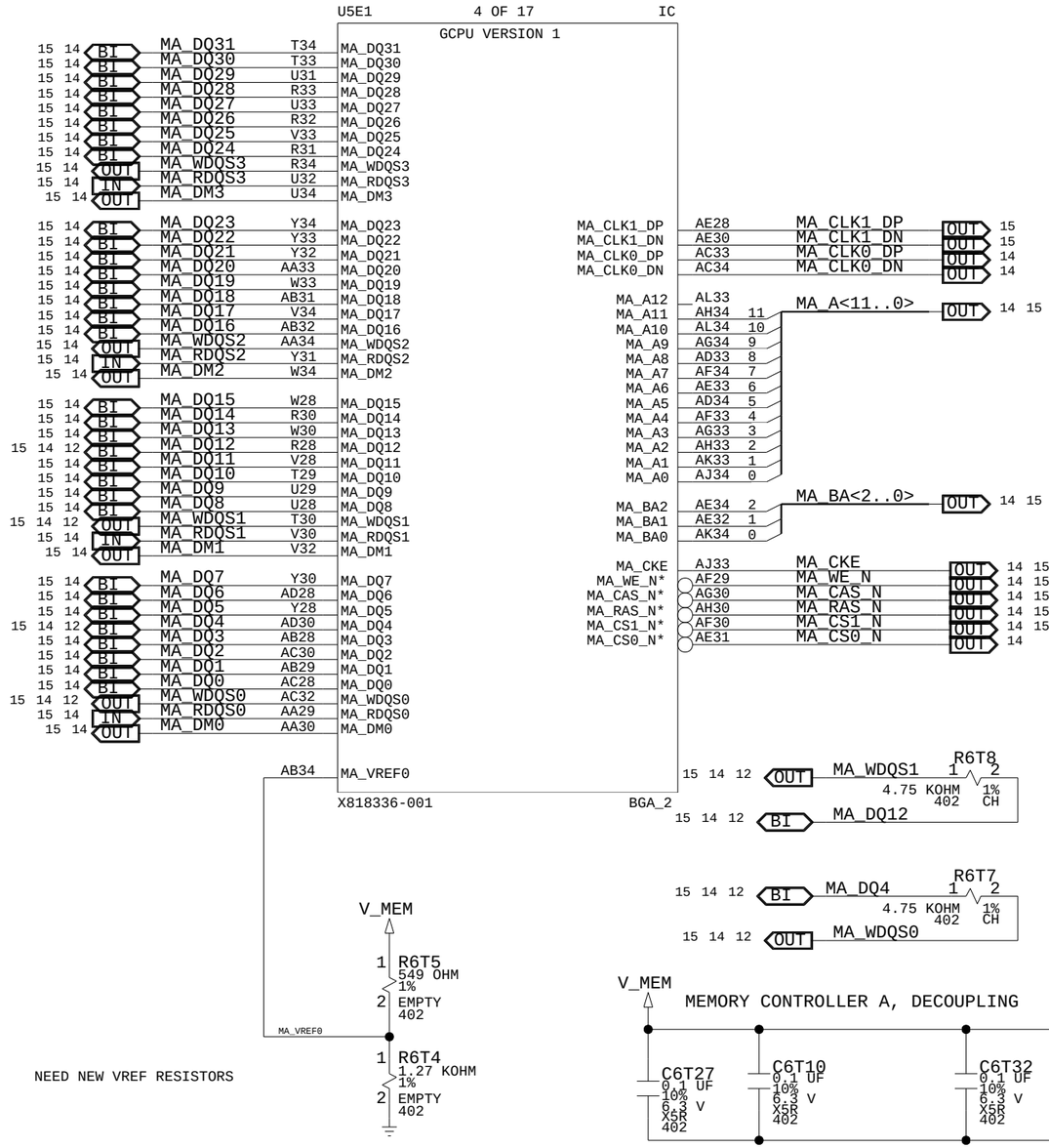
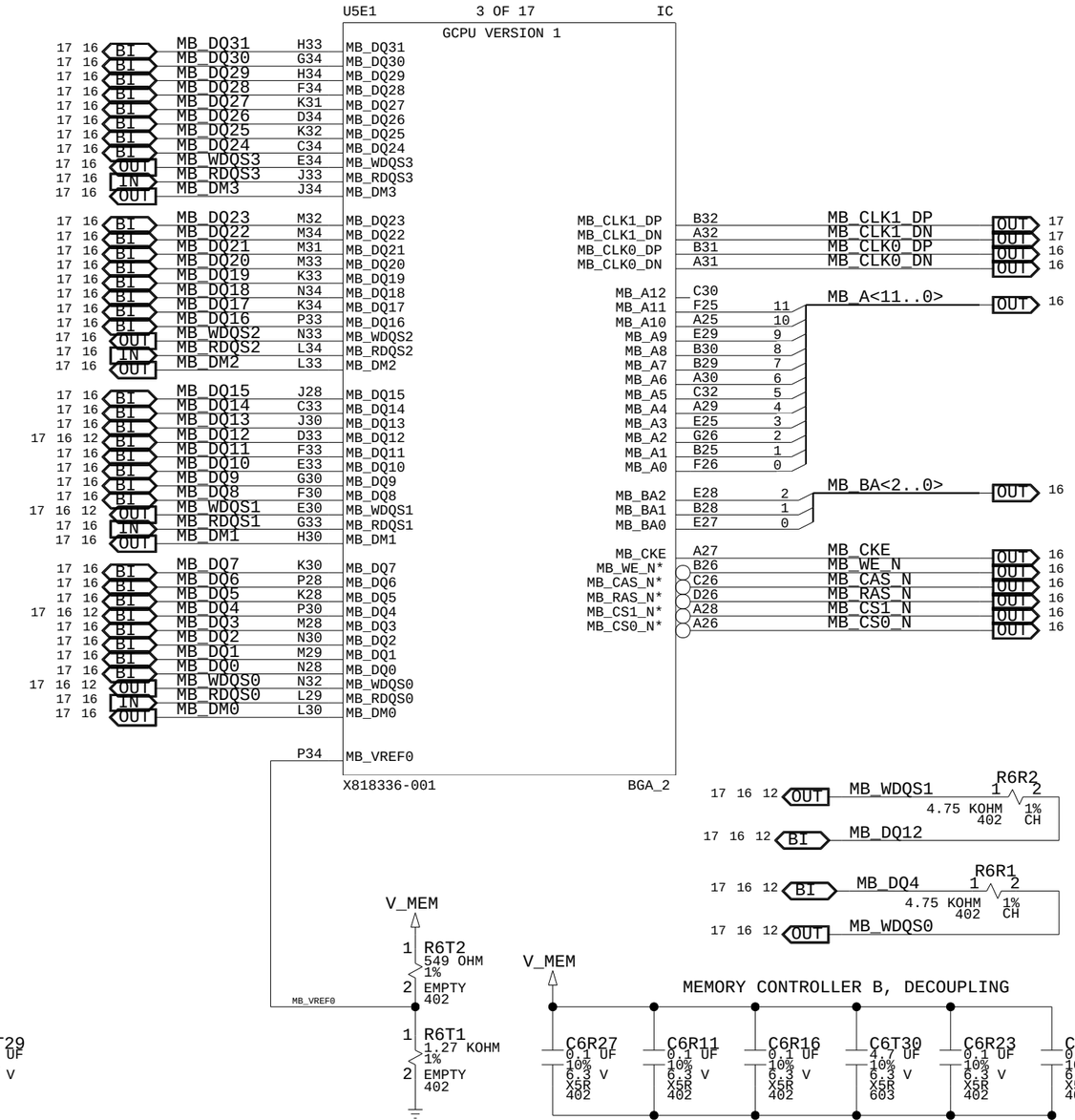
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	11/74	B	1.0

GPU, MEMORY CONTROLLER 0 PARTITION A & B





TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=GPU, MEMORY CONTROLLER A + B]

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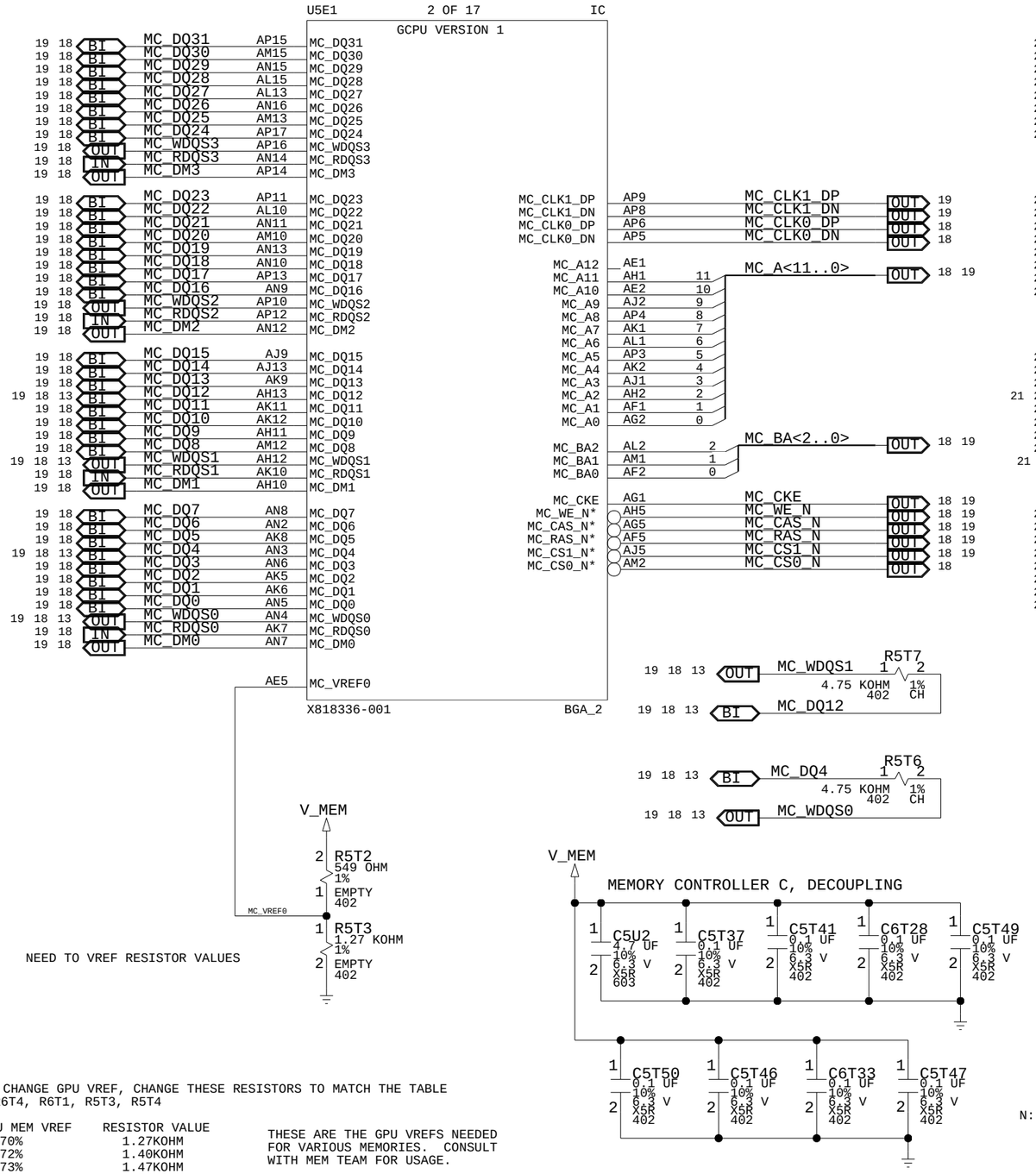
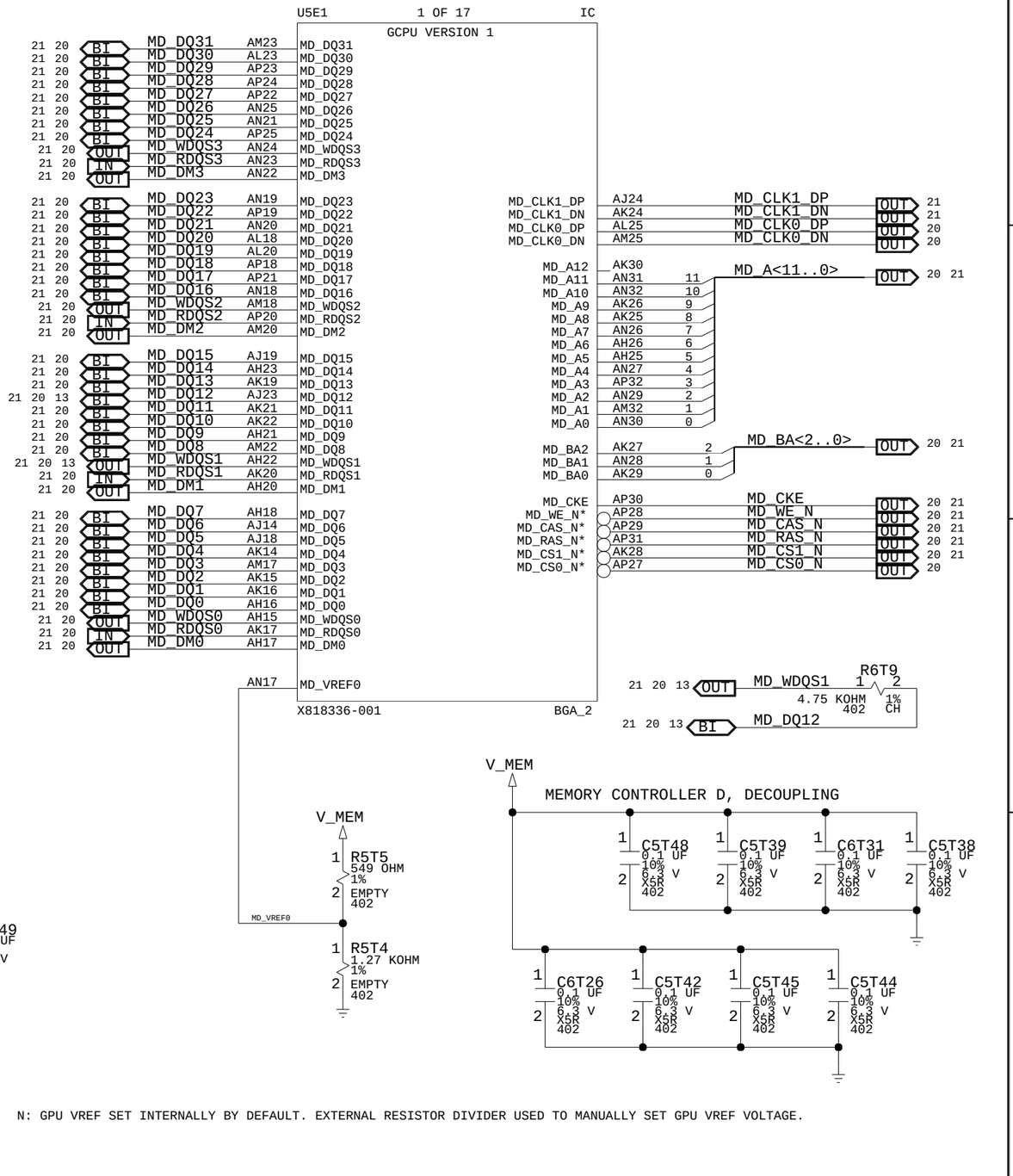
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	12/74	B	1.0

GPU, MEMORY CONTROLLER 1 PARTITION C & D





TO CHANGE GPU VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R6T4, R6T1, R5T3, R5T4

GPU MEM VREF	RESISTOR VALUE
70%	1.27KOHM
72%	1.40KOHM
73%	1.47KOHM
74%	1.54KOHM

THESE ARE THE GPU VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

N: GPU VREF SET INTERNALLY BY DEFAULT. EXTERNAL RESISTOR DIVIDER USED TO MANUALLY SET GPU VREF VOLTAGE.

[PAGE_TITLE=[GPU, MEMORY CONTROLLER C + D]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	13/74	B	1.0

MEMORY PARTITION A, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U7E1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX
U7E1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG PACK_IGNORE=TRUE
U7E1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND PACK_IGNORE=TRUE

V_MEM

R7E5 60.4 OHM 1% CH 402 (1 / 2)

R7E4 60.4 OHM 1% CH 402 (1 / 2)

U7E1 BOM_IGNORE=TRUE EMPTY

GDDR136 (1Gbit) MF=1

12	IN	MA_CLK0_DP	J11	CLK_DP			
12	IN	MA_CLK0_DN	J10	CLK_DN			
19 18 17 16 15 4 21 20	IN	MEM_RST	V9	RESET			
			J2	A12 (1Gbit only, dual-load)			
15 12	IN	MA_A<11..0>	11 L4	A11/A7			
			10 K2	A10/A8			
			9 M9	A9/A3			
			8 K11	A8/A10			
			7 L9	A7/A11			
			6 K10	A6/A2			
			5 H11	A5/A1			
			4 K9	A4/A0			
			3 M4	A3/A9			
			2 K3	A2/A6			
			1 H2	A1/A5			
			0 K4	A0/A4			
15 12	IN	MA_BA<2..0>	2 H10	BA2/RAS_N			
			1 G9	BA1/BA0			
			0 G4	BA0/BA1			
15 12	IN	MA_CKE	H4	CKE/WE_N			
15 12	IN	MA_WE_N	H9	WE_N/CKE			
15 12	IN	MA_CAS_N	F4	CAS_N/CS_N			
15 12	IN	MA_RAS_N	H3	RAS_N/BA2			
12	IN	MA_CS0_N	F9	CS_N/CAS_N			
15 12	IN	MA_CS1_N	J3	CS1_N (1Gbit only, single-load)			
20 18 16 4	IN	MEM_SCAN_TOP_EN	A9	MF			
19 18 17 16 15 4 21 20	IN	MEM_SCAN_EN	V4	SCAN_EN			
15 14	IN	MEM_A_VREF1	H1	VREF1			
15	IN	MEM_A_VREF0	H12	VREF0			
					DQ31	T3	MA_DQ31
					DQ30	T2	MA_DQ30
					DQ29	R3	MA_DQ29
					DQ28	R2	MA_DQ28
					DQ27	M3	MA_DQ27
					DQ26	N2	MA_DQ26
					DQ25	L3	MA_DQ25
					DQ24	M2	MA_DQ24
					WDQS3	P2	MA_WDQS3
					RDQS3	P3	MA_RDQS3
					DM3	N3	MA_DM3
					DQ23	T10	MA_DQ23
					DQ22	T11	MA_DQ22
					DQ21	R10	MA_DQ21
					DQ20	R11	MA_DQ20
					DQ19	M10	MA_DQ19
					DQ18	N11	MA_DQ18
					DQ17	L10	MA_DQ17
					DQ16	M11	MA_DQ16
					WDQS2	P11	MA_WDQS2
					RDQS2	P10	MA_RDQS2
					DM2	N10	MA_DM2
					DQ15	G10	MA_DQ15
					DQ14	F11	MA_DQ14
					DQ13	F10	MA_DQ13
					DQ12	E11	MA_DQ12
					DQ11	C10	MA_DQ11
					DQ10	C11	MA_DQ10
					DQ9	B10	MA_DQ9
					DQ8	B11	MA_DQ8
					WDQS1	D11	MA_WDQS1
					RDQS1	D10	MA_RDQS1
					DM1	E10	MA_DM1
					DQ7	G3	MA_DQ7
					DQ6	F2	MA_DQ6
					DQ5	F3	MA_DQ5
					DQ4	E2	MA_DQ4
					DQ3	C3	MA_DQ3
					DQ2	C2	MA_DQ2
					DQ1	B3	MA_DQ1
					DQ0	B2	MA_DQ0
					WDQS0	D2	MA_WDQS0
					RDQS0	D3	MA_RDQS0
					DM0	E3	MA_DM0
					ZQ	A4	MA_ZQ_TOP

R7E8 243 OHM 1% CH 402 (1 / 2)

X802980-019

V_MEM

U7E1 EMPTY

GDDR136 (1Gbit) MF=0

V1	VDDQ<21>	VSSQ<19>	T12
R12	VDDQ<20>	VSSQ<18>	T9
R9	VDDQ<19>	VSSQ<17>	T4
R4	VDDQ<18>	VSSQ<16>	T1
R1	VDDQ<17>	VSSQ<15>	P12
N12	VDDQ<16>	VSSQ<14>	P9
N9	VDDQ<15>	VSSQ<13>	P4
V12	VDDQ<14>	VSSQ<12>	P1
N4	VDDQ<13>	VSSQ<11>	L11
N1	VDDQ<12>	VSSQ<10>	L2
J9	VDDQ<11>	VSSQ<9>	G11
J4	VDDQ<10>	VSSQ<8>	G2
E12	VDDQ<9>	VSSQ<7>	D12
E9	VDDQ<8>	VSSQ<6>	D9
E4	VDDQ<7>	VSSQ<5>	D4
E1	VDDQ<6>	VSSQ<4>	D1
C12	VDDQ<5>	VSSQ<3>	B12
C9	VDDQ<4>	VSSQ<2>	B9
C4	VDDQ<3>	VSSQ<1>	B4
C1	VDDQ<2>	VSSQ<0>	B1
A12	VDDQ<1>		
A1	VDDQ<0>		
V2	VDD<7>	VSS<7>	V3
M12	VDD<6>	VSS<6>	L12
M1	VDD<5>	VSS<5>	L1
V11	VDD<4>	VSS<4>	G12
F12	VDD<3>	VSS<3>	G1
F1	VDD<2>	VSS<2>	A10
A11	VDD<1>	VSS<1>	V10
A2	VDD<0>	VSS<0>	A3
K12	VDDA<1>		
K1	VDDA<0>		
J12	VSSA<1>		
J1	VSSA<0>		

X802980-019

MX_CS1_N CONNECTED TO J3 TO SUPPORT 1G RAM CONFIGS.

V_MEM

R7T5 549 OHM 1% CH 402 (1 / 2)

MEM_A_VREF1 OUT 14 15

GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND

R7T4 1.27 KOHM 1% CH 402 (1 / 2)

C7T7 0.1 UF 10% 6.3 V X5R 402

TO CHANGE MEM VREF, CHANGE THESE RESISTORS TO MATCH THE TABLE
R7T4, R7E7, R7R4, R7D5, R5U4, R5F2, R6U4, R6F2

MEM VREF	RESISTOR VALUE
69%	1.21KOHM
70%	1.27KOHM
72%	1.40KOHM

THESE ARE THE MEM VREFS NEEDED FOR VARIOUS MEMORIES. CONSULT WITH MEM TEAM FOR USAGE.

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R7T4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE

PARTITION A DECOUPLING

V_MEM

C7E8 4.7 UF 10% 6.3 V X5R 603 (1 / 2)

V_MEM

MEMORY A, TOP, DECOUPLING

C7E14 C7E11 C7E6 C7E5 C7E13 C7E10 C7E4 C7E7 — 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION A, TOP]

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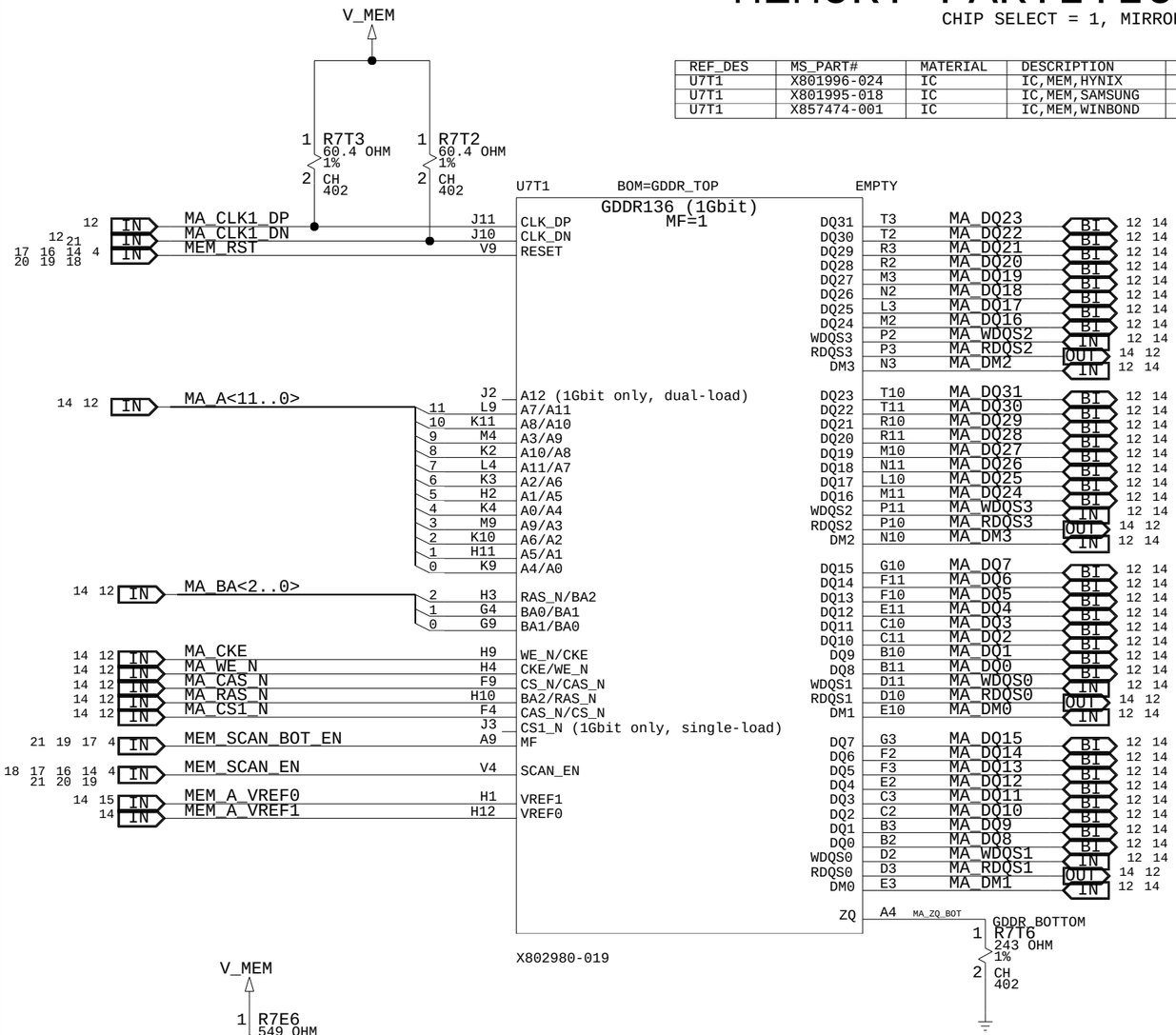
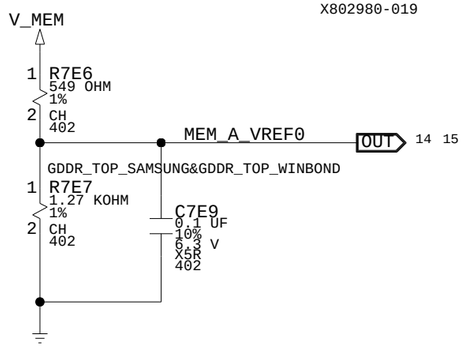
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	14/74	B	1.0

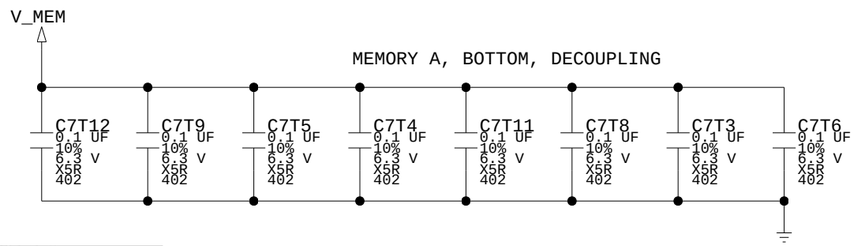
MEMORY PARTITION A, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U7T1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX PACK_IGNORE=TRUE
U7T1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG PACK_IGNORE=TRUE
U7T1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND PACK_IGNORE=TRUE







REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R7E7	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE

[PAGE_TITLE=MEMORY PARTITION A, BOTTOM]

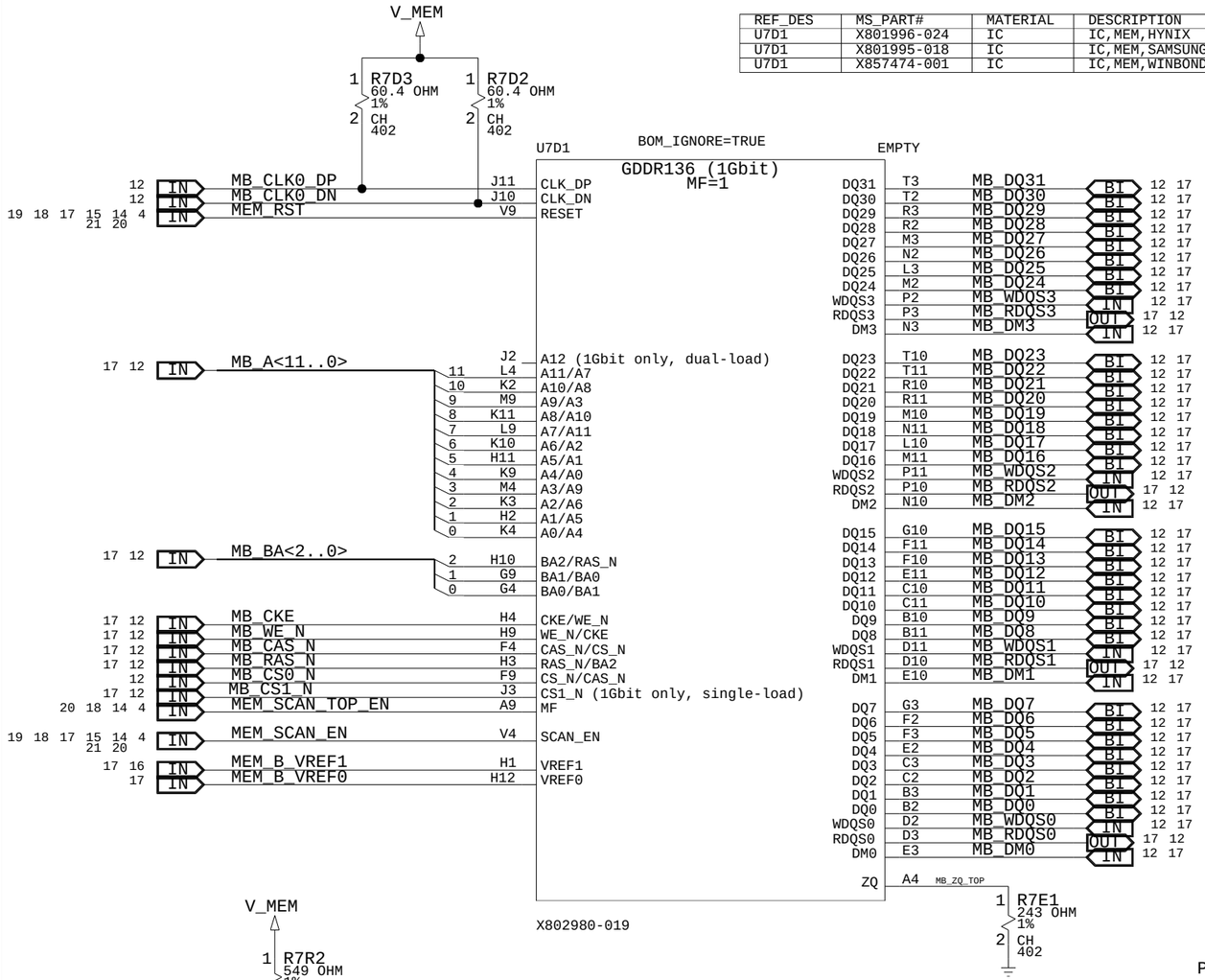
DRAWING
Wed Mar 14 01:47:37 2012

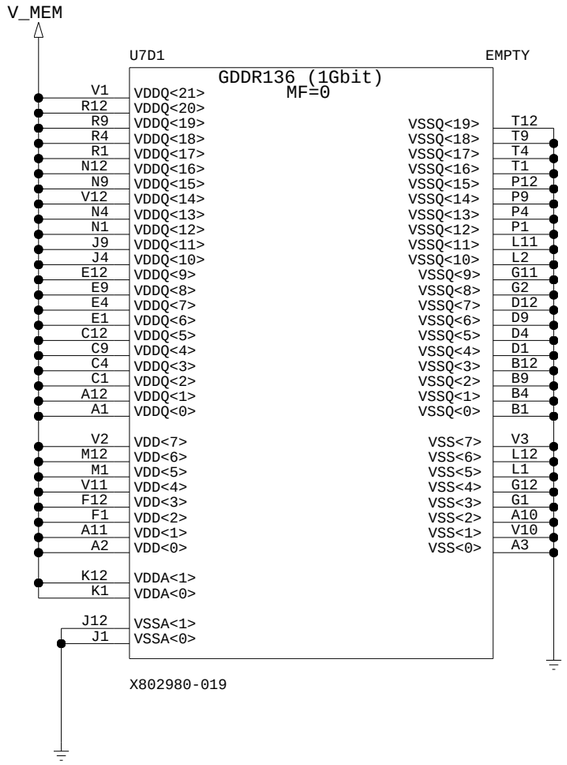
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	15/74	B	1.0

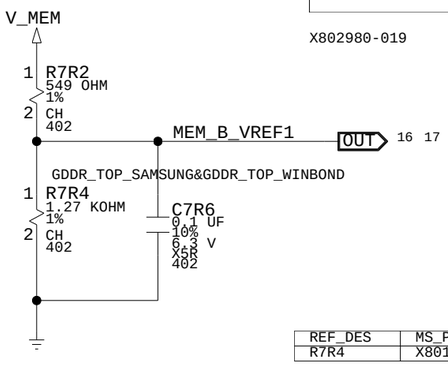
MEMORY PARTITION B, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U7D1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX
U7D1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG, PACK_IGNORE=TRUE
U7D1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND, PACK_IGNORE=TRUE

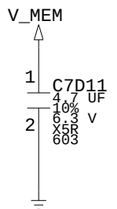


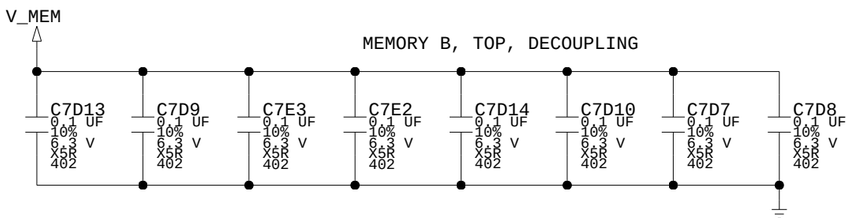




REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R7R4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE

PARTITION B DECOUPLING





[PAGE_TITLE=MEMORY PARITION B, TOP]

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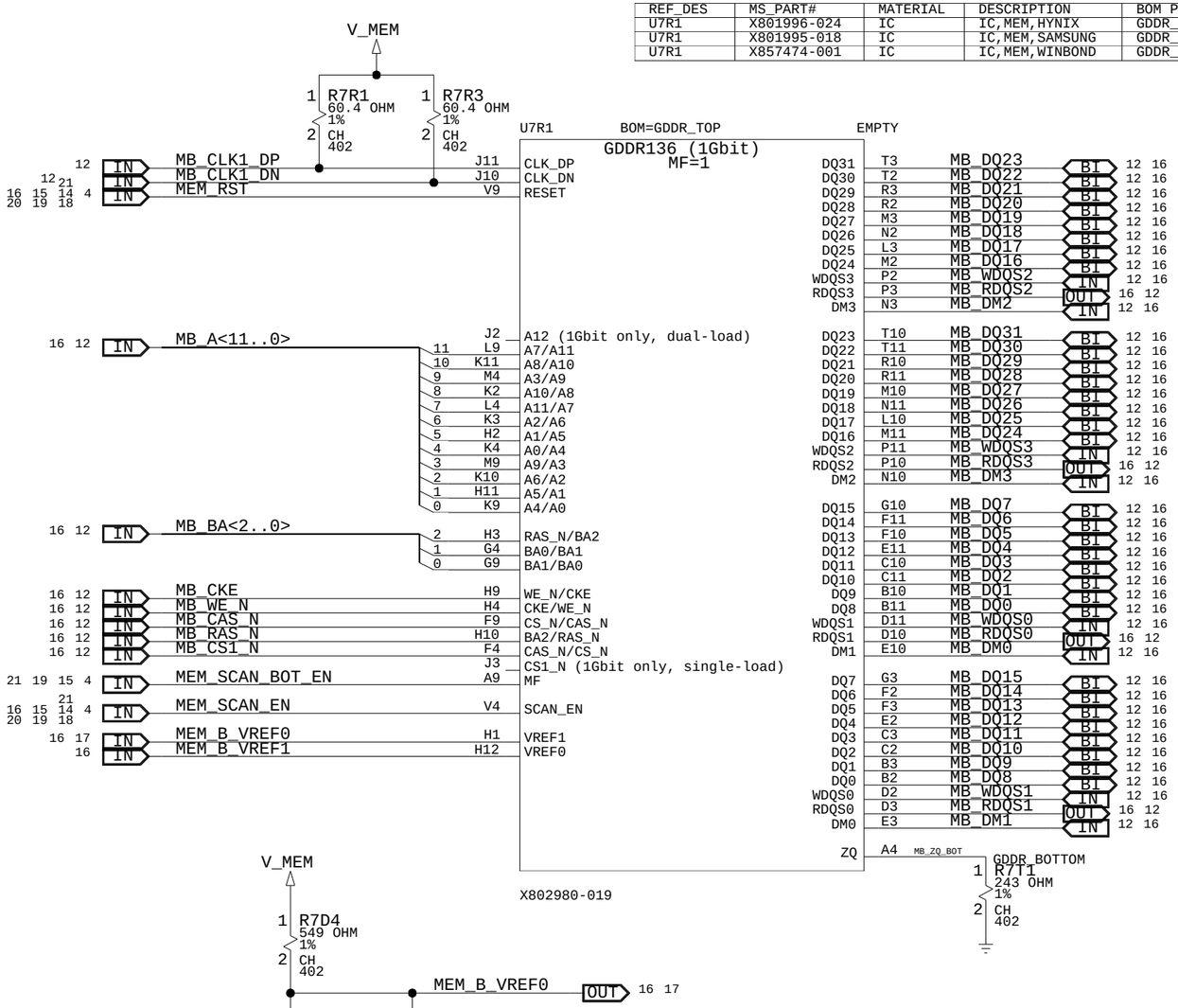
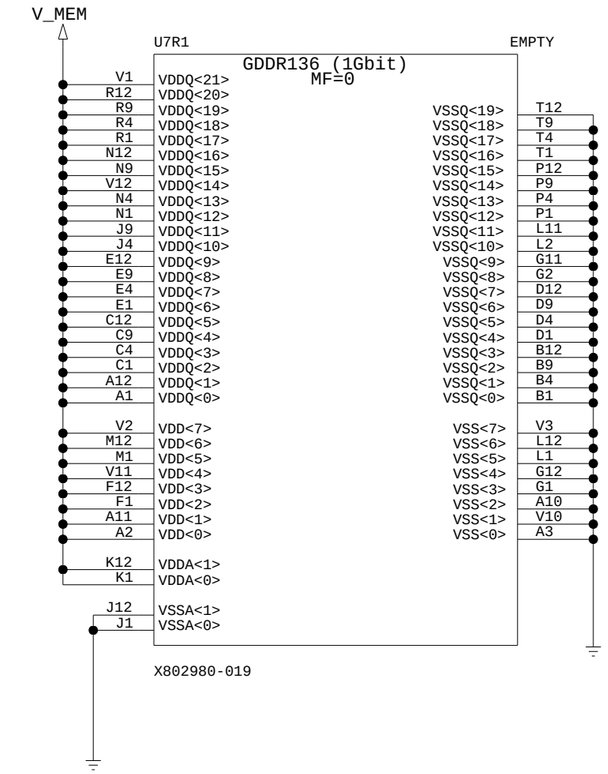
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	16/74	B	1.0

MEMORY PARTITION B, BOTTOM

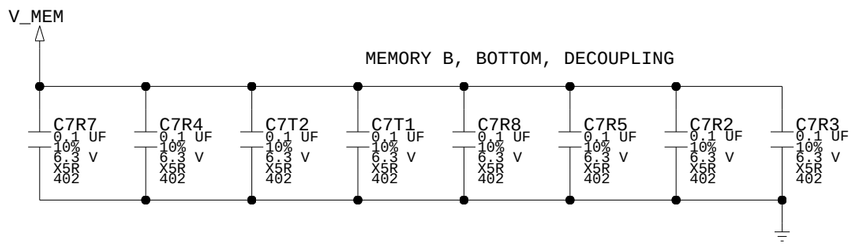
CHIP SELECT = 1, MIRROR FUNCTION = 1

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM_PROPERTY
U7R1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX PACK_IGNORE=TRUE
U7R1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG PACK_IGNORE=TRUE
U7R1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND PACK_IGNORE=TRUE





REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R7D5	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE



[PAGE_TITLE=MEMORY PARITION B, BOTTOM]

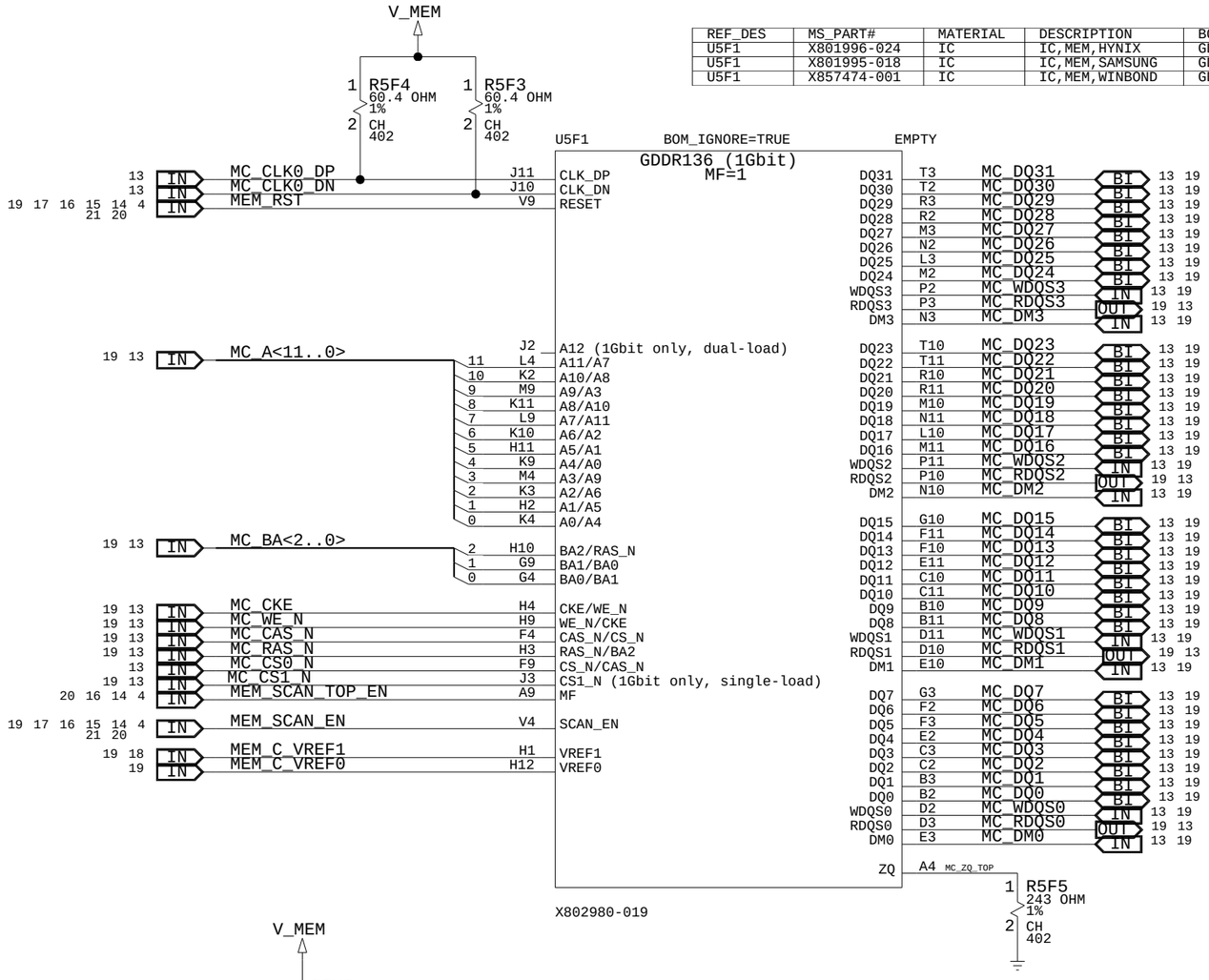
DRAWING
Wed Mar 14 01:47:39 2012

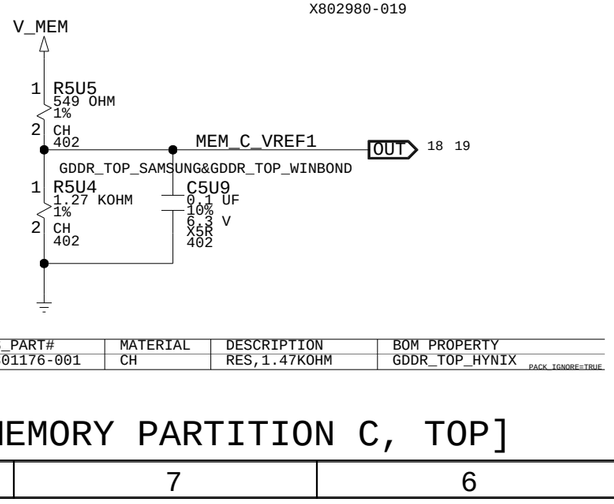
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	17/74	B	1.0

MEMORY PARTITION C, TOP

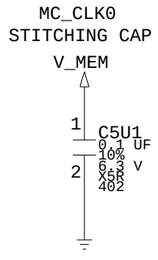
CHIP SELECT = 0, MIRROR FUNCTION = 0

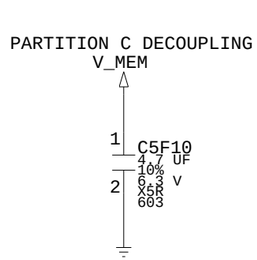
REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U5F1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX PACK_IGNORE=TRUE
U5F1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG PACK_IGNORE=TRUE
U5F1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND PACK_IGNORE=TRUE

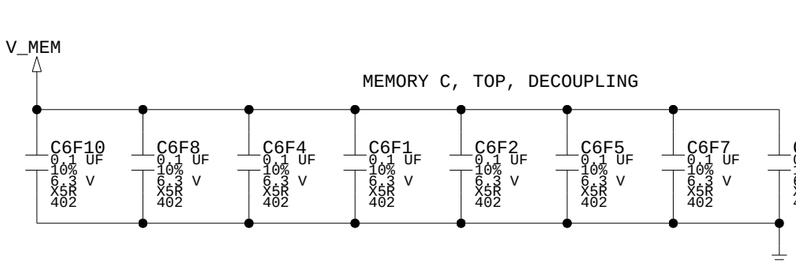




REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R5U4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE







[PAGE_TITLE=MEMORY PARTITION C, TOP]

DRAWING
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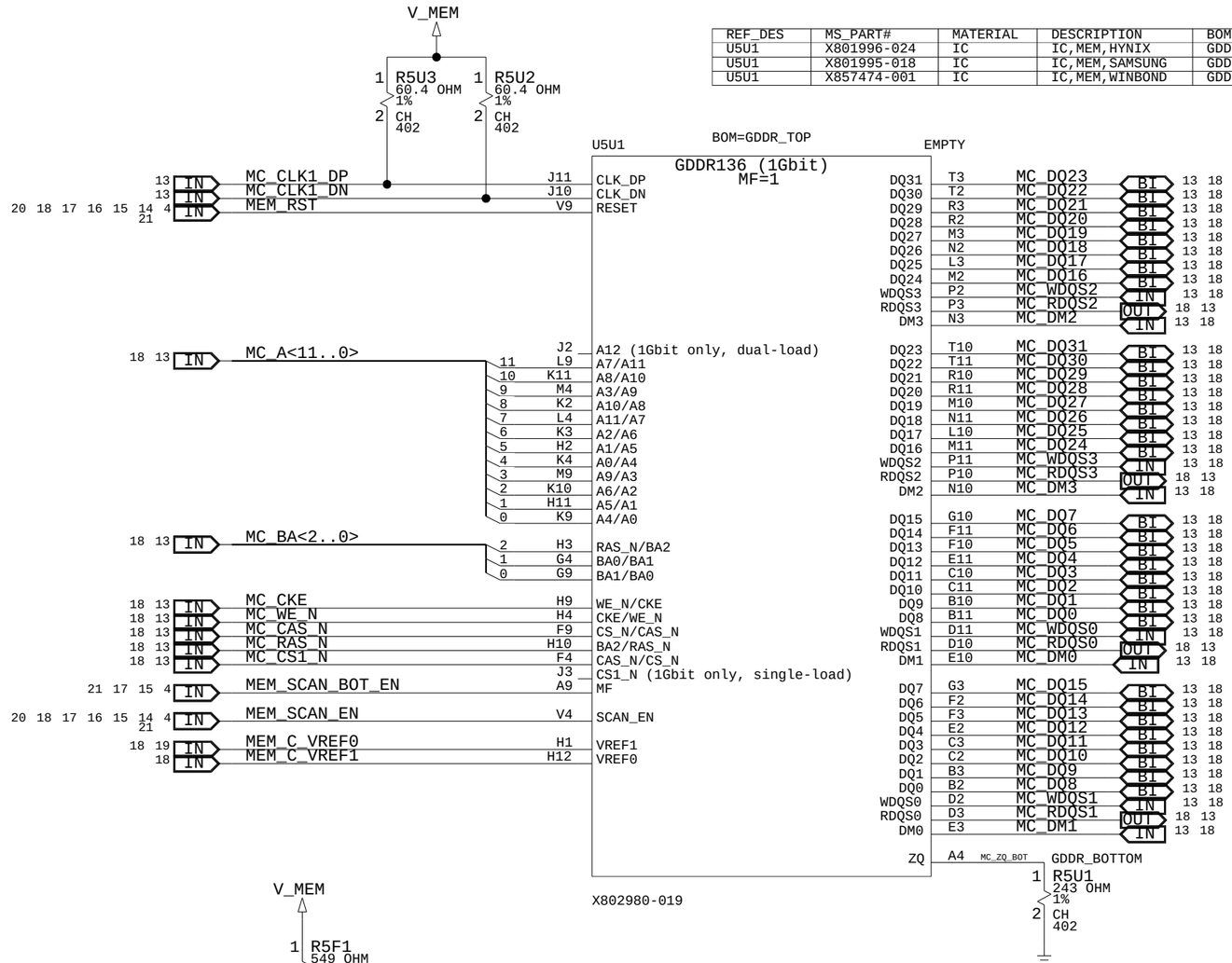
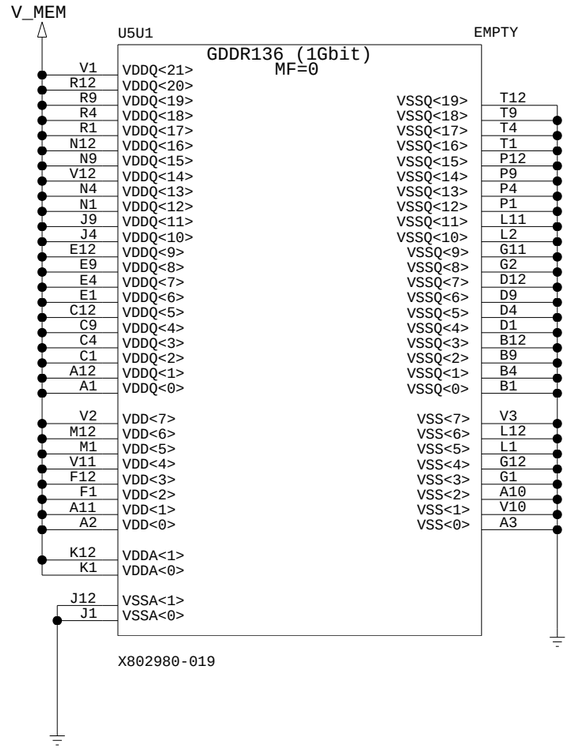
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	18/74	B	1.0

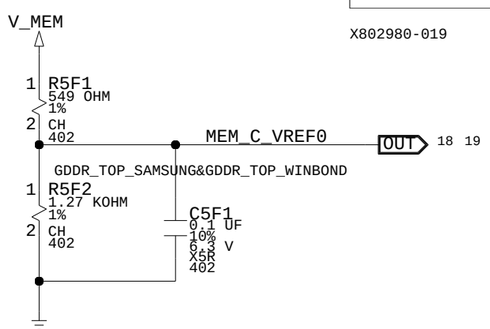
MEMORY PARTITION C, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

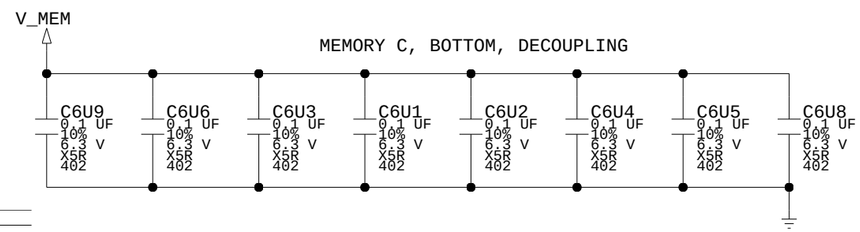
REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U5U1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX
U5U1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG PACK_IGNORE=TRUE
U5U1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND PACK_IGNORE=TRUE







REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R5F2	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE



[PAGE_TITLE=MEMORY PARITION C, BOTTOM]

DRAWING
Wed Mar 14 01:47:40 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	19/74	B	1.0

MEMORY PARTITION D, TOP

CHIP SELECT = 0, MIRROR FUNCTION = 0

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U6F1	X801996-024	IC	IC,MEM,HYNIX	GDDR_TOP_HYNIX
U6F1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_TOP_SAMSUNG PACK_IGNORE=TRUE
U6F1	X857474-001	IC	IC,MEM,WINBOND	GDDR_TOP_WINBOND PACK_IGNORE=TRUE

V_MEM

R6F4 60.4 OHM 1% CH 402 (1 / 2)

R6F3 60.4 OHM 1% CH 402 (1 / 2)

U6F1 BOM_IGNORE=TRUE — GDDR136 (1Gbit) MF=1

13	IN	MD_CLK0_DP	J11	CLK_DP			
13	IN	MD_CLK0_DN	J10	CLK_DN			
18 17 16 15 14 4 21 19	IN	MEM_RST	V9	RESET			
			J2	A12 (1Gbit only, dual-load)			
21 13	IN	MD_A<11..0>	11 L4	A11/A7			
			10 K2	A10/A8			
			9 M9	A9/A3			
			8 K11	A8/A10			
			7 L9	A7/A11			
			6 K10	A6/A2			
			5 H11	A5/A1			
			4 K9	A4/A0			
			3 M4	A3/A9			
			2 K3	A2/A6			
			1 H2	A1/A5			
			0 K4	A0/A4			
21 13	IN	MD_BA<2..0>	2 H10	BA2/RAS_N			
			1 G9	BA1/BA0			
			0 G4	BA0/BA1			
21 13	IN	MD_CKE	H4	CKE/WE_N			
21 13	IN	MD_WE_N	H9	WE_N/CKE			
21 13	IN	MD_CAS_N	F4	CAS_N/CS_N			
21 13	IN	MD_RAS_N	H3	RAS_N/BA2			
13	IN	MD_CS0_N	F9	CS_N/CAS_N			
21 13	IN	MD_CS1_N	J3	CS1_N (1Gbit only, single-load)			
18 16 14 4	IN	MEM_SCAN_TOP_EN	A9	MF			
18 17 16 15 14 4 21 19	IN	MEM_SCAN_EN	V4	SCAN_EN			
21 20	IN	MEM_D_VREF1	H1	VREF1			
21	IN	MEM_D_VREF0	H12	VREF0			

					DQ31	T3	MD_DQ31 BI 13 21
					DQ30	T2	MD_DQ30 BI 13 21
					DQ29	R3	MD_DQ29 BI 13 21
					DQ28	R2	MD_DQ28 BI 13 21
					DQ27	M3	MD_DQ27 BI 13 21
					DQ26	N2	MD_DQ26 BI 13 21
					DQ25	L3	MD_DQ25 BI 13 21
					DQ24	M2	MD_DQ24 BI 13 21
					WDQS3	P2	MD_WDQS3 IN 13 21
					RDQS3	P3	MD_RDQS3 OUT 21 13
					DM3	N3	MD_DM3 IN 13 21
					DQ23	T10	MD_DQ23 BI 13 21
					DQ22	T11	MD_DQ22 BI 13 21
					DQ21	R10	MD_DQ21 BI 13 21
					DQ20	R11	MD_DQ20 BI 13 21
					DQ19	M10	MD_DQ19 BI 13 21
					DQ18	N11	MD_DQ18 BI 13 21
					DQ17	L10	MD_DQ17 BI 13 21
					DQ16	M11	MD_DQ16 BI 13 21
					WDQS2	P11	MD_WDQS2 IN 13 21
					RDQS2	P10	MD_RDQS2 OUT 21 13
					DM2	N10	MD_DM2 IN 13 21
					DQ15	G10	MD_DQ15 BI 13 21
					DQ14	F11	MD_DQ14 BI 13 21
					DQ13	F10	MD_DQ13 BI 13 21
					DQ12	E11	MD_DQ12 BI 13 21
					DQ11	C10	MD_DQ11 BI 13 21
					DQ10	C11	MD_DQ10 BI 13 21
					DQ9	B10	MD_DQ9 BI 13 21
					DQ8	B11	MD_DQ8 BI 13 21
					WDQS1	D11	MD_WDQS1 IN 13 21
					RDQS1	D10	MD_RDQS1 OUT 21 13
					DM1	E10	MD_DM1 IN 13 21
					DQ7	G3	MD_DQ7 BI 13 21
					DQ6	F2	MD_DQ6 BI 13 21
					DQ5	F3	MD_DQ5 BI 13 21
					DQ4	E2	MD_DQ4 BI 13 21
					DQ3	C3	MD_DQ3 BI 13 21
					DQ2	C2	MD_DQ2 BI 13 21
					DQ1	B3	MD_DQ1 BI 13 21
					DQ0	B2	MD_DQ0 BI 13 21
					WDQS0	D2	MD_WDQS0 IN 13 21
					RDQS0	D3	MD_RDQS0 OUT 21 13
					DM0	E3	MD_DM0 IN 13 21
					ZQ	A4	MD_ZQ_TOP

X802980-019

R6F5 243 OHM 1% CH 402 (1 / 2)

V_MEM

R6U5 549 OHM 1% CH 402 (1 / 2)

MEM_D_VREF1 OUT 20 21

GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND

R6U4 1.27 KOHM 1% CH 402 (1 / 2)

C6U7 0.1 UF 10% 6.3 V X5R 402

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R6U4	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE

V_MEM

U6F1 — GDDR136 (1Gbit) MF=0 — EMPTY

V1	VDDQ<21>	VSSQ<19>	T12
R12	VDDQ<20>	VSSQ<18>	T9
R9	VDDQ<19>	VSSQ<17>	T4
R4	VDDQ<18>	VSSQ<16>	T1
R1	VDDQ<17>	VSSQ<15>	P12
N12	VDDQ<16>	VSSQ<14>	P9
N9	VDDQ<15>	VSSQ<13>	P4
V12	VDDQ<14>	VSSQ<12>	P1
N4	VDDQ<13>	VSSQ<11>	L11
N1	VDDQ<12>	VSSQ<10>	L2
J9	VDDQ<11>	VSSQ<9>	G11
J4	VDDQ<10>	VSSQ<8>	G2
E12	VDDQ<9>	VSSQ<7>	D12
E9	VDDQ<8>	VSSQ<6>	D9
E4	VDDQ<7>	VSSQ<5>	D4
E1	VDDQ<6>	VSSQ<4>	D1
C12	VDDQ<5>	VSSQ<3>	B12
C9	VDDQ<4>	VSSQ<2>	B9
C4	VDDQ<3>	VSSQ<1>	B4
C1	VDDQ<2>	VSSQ<0>	B1
A12	VDDQ<1>		
A1	VDDQ<0>		
V2	VDD<7>	VSS<7>	V3
M12	VDD<6>	VSS<6>	L12
M1	VDD<5>	VSS<5>	L1
V11	VDD<4>	VSS<4>	G12
F12	VDD<3>	VSS<3>	G1
F1	VDD<2>	VSS<2>	A10
A11	VDD<1>	VSS<1>	V10
A2	VDD<0>	VSS<0>	A3
K12	VDDA<1>		
K1	VDDA<0>		
J12	VSSA<1>		
J1	VSSA<0>		

X802980-019

PARTITION D DECOUPLING

V_MEM

C6F11 4.7 UF 10% 6.3 V X5R 603 (1 / 2)

V_MEM

MEMORY D, TOP, DECOUPLING

C5F9 0.1 UF 10% 6.3 V X5R 402

C5F7 0.1 UF 10% 6.3 V X5R 402

C5F4 0.1 UF 10% 6.3 V X5R 402

C5F3 0.1 UF 10% 6.3 V X5R 402

C5F2 0.1 UF 10% 6.3 V X5R 402

C5F5 0.1 UF 10% 6.3 V X5R 402

C5F6 0.1 UF 10% 6.3 V X5R 402

C5F8 0.1 UF 10% 6.3 V X5R 402

[PAGE_TITLE=MEMORY PARTITION D, TOP]

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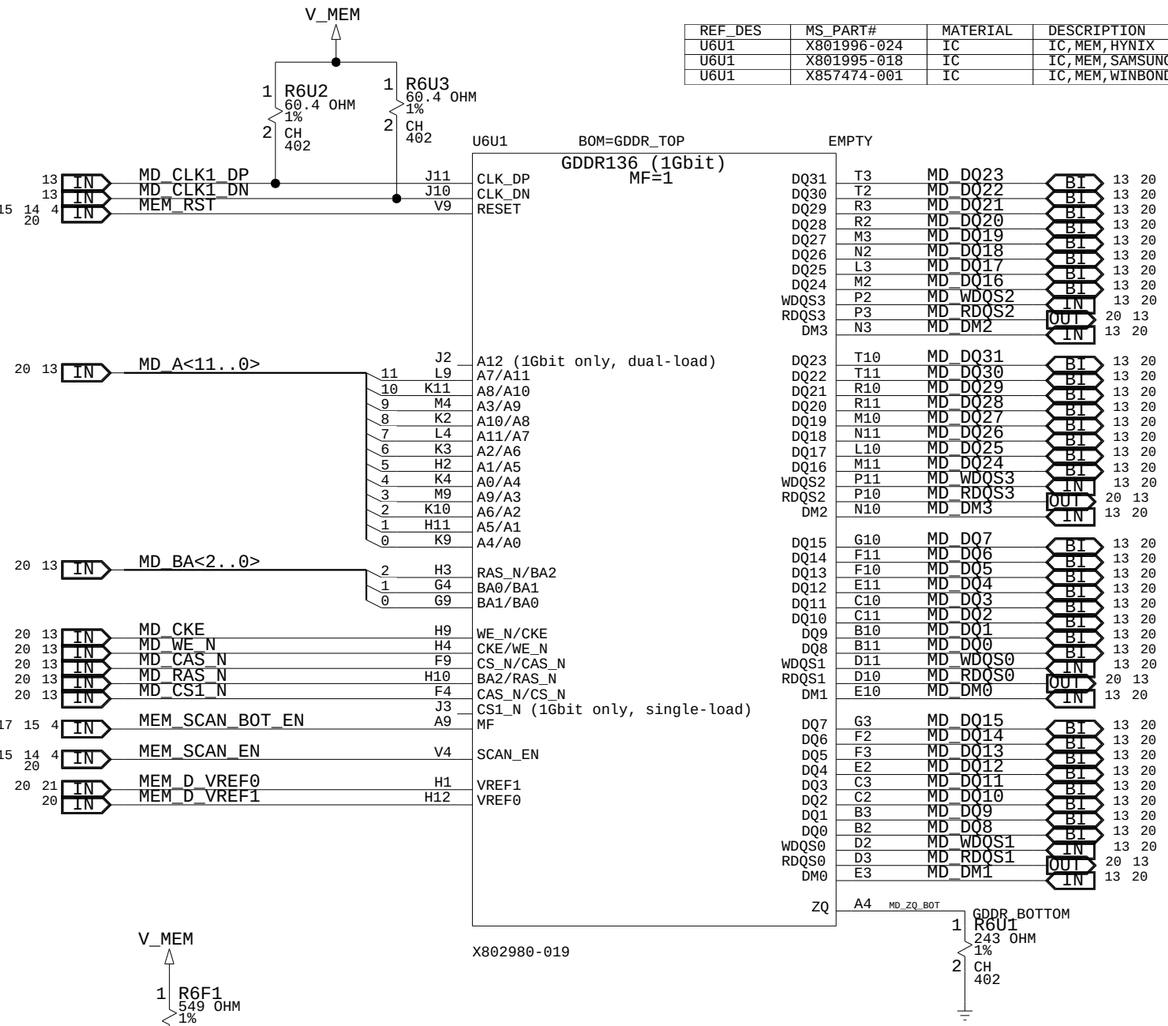
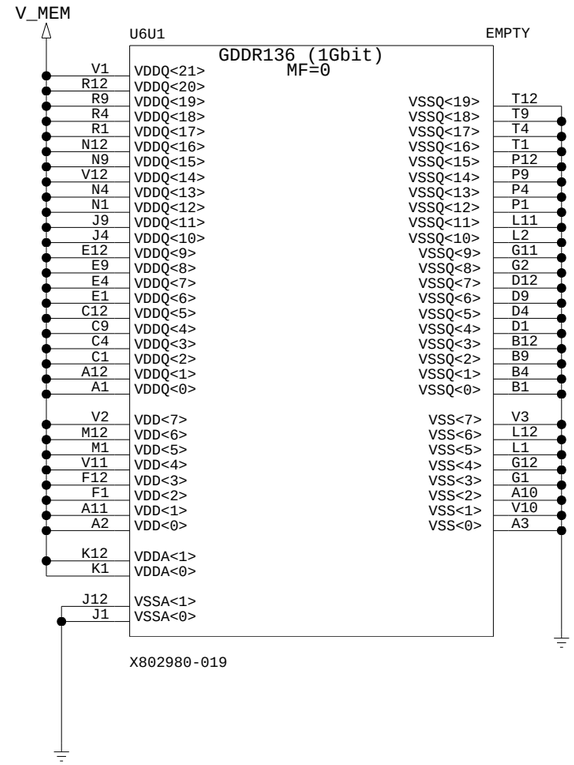
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	20/74	B	1.0

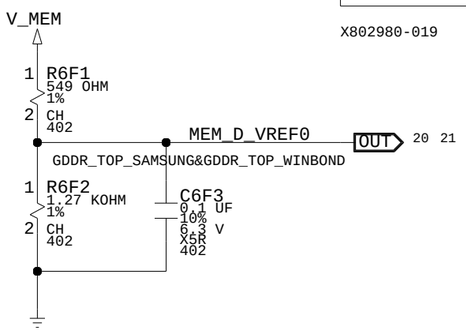
MEMORY PARTITION D, BOTTOM

CHIP SELECT = 1, MIRROR FUNCTION = 1

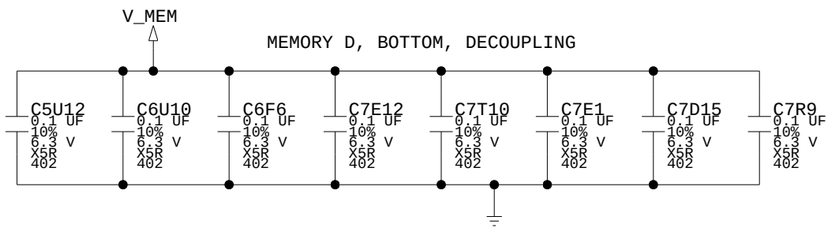
REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U6U1	X801996-024	IC	IC,MEM,HYNIX	GDDR_BOT_HYNIX PACK_IGNORE=TRUE
U6U1	X801995-018	IC	IC,MEM,SAMSUNG	GDDR_BOT_SAMSUNG PACK_IGNORE=TRUE
U6U1	X857474-001	IC	IC,MEM,WINBOND	GDDR_BOT_WINBOND PACK_IGNORE=TRUE

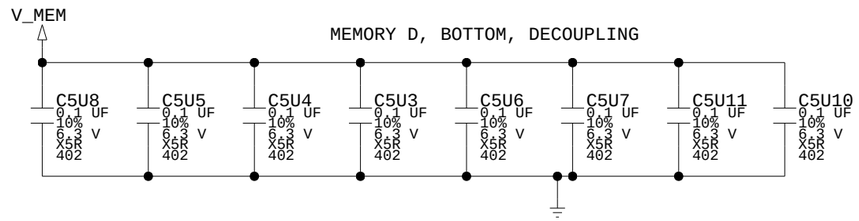






REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R6F2	X801176-001	CH	RES,1.47KOHM	GDDR_TOP_HYNIX PACK_IGNORE=TRUE





[PAGE_TITLE=MEMORY PARTITION D, BOTTOM]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	21/74	B	1.0

KSB, CLOCKS + STRAPPING + POR

XTAL BYPASS: STUFF R3, R4, R5, AND C153 AND
APPLY SQUARE WAVE TO XTAL_IN (VL=0V VH=1V)
KEEP R5 CLOSE TO KSB CHIP

RESISTOR VALUES CHOSEN TO GIVE V_12P0_DET 1P8V NOMINAL

V_12P0
V_3P3STBY
V_3P3

DB3D2
Y3D1 25 MHZ SM XTAL
C3D7 27 PF 5% 50 V COG 402
C3D8 22 PF 5% 50 V NPO 402
R3D26 49.9 OHM 1% EMPTY 402
R3R5 1% 84.5 KOHM CH 402
R3R17 1% 15 KOHM CH 402
C3R55 470 PF 5% 50 V EMPTY 402
R3D17 8.25 KOHM 1% EMPTY 402
R3D19 1.5 KOHM 1% EMPTY 402
C3D1 0.01 UF 10% 16 V EMPTY 402

DB2C2
V_12P0_DET
POR_BYPASS

XTAL_IN
XTAL_OUT

DB3D3
DB3D1
EXT_CLK48_IN
EXT_CLK48_SEL

62 61 55 25 BI SMB_DATA
62 61 55 25 BI SMB_CLK

U3D1 KSB IC
1 OF 9
X850744-001 PBGA404 I155

V_12P0_DET	W20	V_12P0_DET
POR_BYPASS	B4	POR_BYPASS<DN>
	AB21	XTAL_IN
	AA21	XTAL_OUT
	AA22	XTAL_VSS
	Y20	CLK48<DN>
	W19	CLK48_BYPASS<DN>
	A4	SMB_DATA
	A5	SMB_CLK

SB_KSB_BASE

V_12P0_OK	C5	V12P0_PWRGD → OUT 25 42
V_RST_OK<DN>	V19	V_RST_OK → OUT; FTP FT3R3
MAIN_PWR_OK	C4	SB_MAIN_PWRGD ← IN 25; FTP FT3P5
SB_RST_N*	C9	SB_RST_N_R → R3P2 1 KOHM 402 5% CH; R2P3 10 KOHM 5% CH 402; SB_RST_N ← IN 25
SMC_RST_N_OUT	D7	SMC_RST_N_R → R3P15 10 KOHM 5% CH 402; R3P16 1 KOHM 402 5% CH; SMC_RST_N → OUT 25 42 62
CPU_CLK_DP	U21	CPU_CLK_DP_R → R3D6 33 OHM 402 5% CH; R3D7 49.9 OHM 402 1% CH; CPU_CLK_DP → OUT 2
CPU_CLK_DN	V21	CPU_CLK_DN_R → R3D8 33 OHM 402 5% CH; R3D9 49.9 OHM 402 1% CH; CPU_CLK_DN → OUT 2
NB_CLK_DP	V22	GPU_CLK_DP_R → R3D10 33 OHM 402 5% CH; R3D11 49.9 OHM 402 1% CH; GPU_CLK_DP → OUT 4 62
NB_CLK_DN	W22	GPU_CLK_DN_R → R3D12 33 OHM 402 5% CH; R3D13 49.9 OHM 402 1% CH; GPU_CLK_DN → OUT 4 62
PCIEX_CLK_IN_DP	Y15	EXT_PCIEX_CLK_DP
PCIEX_CLK_IN_DN	AA15	EXT_PCIEX_CLK_DN
PIX_CLK_OUT_DP	U22	PIX_CLK_2X_DP_R → R3D5 33 OHM 402 5% CH; R3D14 60.4 OHM 402 1% CH; PIX_CLK_2X_DP → OUT 4; FTP FT3R7
PIX_CLK_OUT_DN	T22	PIX_CLK_2X_DN_R → R3D3 33 OHM 402 5% CH; R3D4 60.4 OHM 402 1% CH; PIX_CLK_2X_DN → OUT 4; FTP FT3R2

V_3P3 → R3D28 10 KOHM 1% CH 402; R3D29 10 KOHM 1% CH 402; DB3R6; DB3R7

I2C ADDRESS

	0011 100 R/W HEX	0111 000 R/W HEX
WRITE	0011 100 0 0X38	0111 000 0 0X70
READ	0011 100 1 0X39	0111 000 1 0X71

	0011 110 R/W HEX
WRITE	0011 110 0 0X3C
READ	0011 110 1 0X3D

[PAGE_TITLE=KSB, CLOCKS + STRAPING]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	22/74	B	1.0

KSB, VIDEO + FAN

U3D1 KSB IC

2 OF 9

4 IN GPU_PIX_CLK_1X → J20 PIX_CLK_IN

4 IN PIX_DATA<14..0>

14	G20	PIX_DATA14
13	G21	PIX_DATA13
12	G22	PIX_DATA12
11	H20	PIX_DATA11
10	H21	PIX_DATA10
9	H22	PIX_DATA9
8	J21	PIX_DATA8
7	J22	PIX_DATA7
6	K21	PIX_DATA6
5	K22	PIX_DATA5
4	K20	PIX_DATA4
3	L21	PIX_DATA3
2	L22	PIX_DATA2
1	L20	PIX_DATA1
0	M20	PIX_DATA0

4 IN GPU_HSYNC_OUT → M22 HSYNC_IN

4 IN GPU_VSYNC_OUT → M21 VSYNC_IN

DAC_RSET → D20 DAC_RSET

1 R3P11 5.11 KOHM 0.1% 2 CH 402

DAC_D_OUT_DP A20 VID_DACD_DP → OUT 37

DAC_D_OUT_DN F18

DAC_B_OUT_DP A21 VID_DACB_DP → OUT 37

DAC_B_OUT_DN G18

DAC_A_OUT_DP C22 VID_DACA_DP → OUT 37

DAC_A_OUT_DN G19

DAC_C_OUT_DP D22 VID_DACC_DP → OUT 37

DAC_C_OUT_DN H18

HSYNC_OUT B19 VID_HSYNC_OUT_R → OUT 37

VSYNC_OUT C19 VID_VSYNC_OUT_R → OUT 37

38 61 IN BRD_TEMP_P — R4G2 0 OHM 5% 402 EMPTY — BRD_TEMP_P_DIODE — Q4G1 EMPTY

61 38 OUT BRD_TEMP_N — R4G1 0 OHM 5% 402 EMPTY — BRD_TEMP_N_DIODE

40 IN HDMI_HPD → D18 HDMI_HPD

KSB_RSET → H4 RSET

1 R2P4 2 KOHM 1% 2 CH 402

FT3P1 FTP 1

25 IN SMC_PWM0 — R3P3 205 KOHM 1% 402 EMPTY — FAN_OP1_DP → F22 FAN_OP1_DP

C3P2 0.22 UF 10% 6.3 V EMPTY 402

66 61 IN CPU_TEMP_N_KSB — ST3C5 SHORT

66 61 IN GPU_TEMP_N_KSB — ST3C2 SHORT

66 61 IN EDRAM_TEMP_N_KSB — ST3C4 SHORT

61 IN BRD_TEMP_N_KSB — ST3C3 SHORT

23 IN CAL_TEMP_N — ST3C1 SHORT

36 IN FAN1_FDBK → F21 FAN_OP1_DN

P22 TEMP_N

TMDS_TXC_DP A16 HDMI_TXC_DP — C3C4 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TXC_DP_R — R3C23 301 OHM 603 1% EMPTY → OUT 40

TMDS_TXC_DN B16 HDMI_TXC_DN → OUT 40

TMDS_TX2_DP B13 HDMI_TX2_DP — C3C1 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX2_DP_R — R3C20 301 OHM 603 1% EMPTY → OUT 40

TMDS_TX2_DN C13 HDMI_TX2_DN → OUT 40

TMDS_TX1_DP A14 HDMI_TX1_DP — C3C2 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX1_DP_R — R3C21 301 OHM 603 1% EMPTY → OUT 40

TMDS_TX1_DN B14 HDMI_TX1_DN → OUT

TMDS_TX0_DP B15 HDMI_TX0_DP — C3C3 0.1 UF 10% 6.3 V EMPTY 402 — HDMI_TX0_DP_R — R3C22 301 OHM 603 1% EMPTY → OUT 40

TMDS_TX0_DN C15 HDMI_TX0_DN → OUT 40

DDC_SCK A12 HDMI_DDC_CLK ↔ BI 37 40 55

DDC_SDA B12 HDMI_DDC_DATA ↔ BI 37 40 55

DB3P1 DB3R1 DB3P2 DB3R2 — CUSTOM THERMAL CALIBRATION PADS LOCATION MUST REMAIN LOCKED

FAN_OUT1 E21 FAN1_OUT → OUT 36

C3R1 100 PF 5% 50 V EMPTY 402

TEMP3_P N22 CAL_TEMP_P — CAL_TEMP_N → OUT 23

TEMP2_P P20 — GPU_TEMP_P_KSB → OUT 61 66

TEMP1_P P21 — CPU_TEMP_P_KSB → OUT 61 66

TEMP0_P R21 — EDRAM_TEMP_P_KSB → OUT 61 66

TEMP4_P N21 — BRD_TEMP_P_KSB → OUT 61

X850744-001 PBGA404

[PAGE_TITLE=KSB, VIDEO + FAN]

DRAWING

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	23/74	B	1.0

KSB, PCIEX + SMM GPIO + JTAG

V_3P3

RETAIL

R2C14 10 KOHM 5% EMPTY 402
R2C12 10 KOHM 5% CH 402
R2C18 10 KOHM 5% EMPTY 402
R2C16 10 KOHM 5% EMPTY 402
R2C20 10 KOHM 5% EMPTY 402

DEVKIT

R2C13 1 KOHM 5% CH 402
R2C11 1 KOHM 5% CH 402
R2C17 1 KOHM 5% CH 402
R2C15 1 KOHM 5% CH 402
R2C19 1 KOHM 5% CH 402

DEBUG OUTPUT DISABLED = SB_GPIO<1> HIGH

SB_GPIO<0..15> BI 24 62

GPIO<1> = 0 ENABLE DEBUG OUTPUT
1 DISABLE DEBUG OUTPUT

GPIO<0,2,3> = 111 XENON
110 ZEPHYR A
101 ZEPHYR B
100 ZEPHYR C
011 FALCON
010 JASPER
001 TRINITY
000 CORONA

U3D1 KSB IC

4 OF 9

X850744-001 PBGA404

62 4 IN	PEX_GPU_SB_L1_DP	Y18	PEX_RX1_DP	PEX_TX1_DP	AA19 PEX_SB_GPU_L1_DP_C → C3D5 0.1 UF 10% 6.3 V X5R 402 → PEX_SB_GPU_L1_DP OUT 4 62
62 4 IN	PEX_GPU_SB_L1_DN	AA18	PEX_RX1_DN	PEX_TX1_DN	AB19 PEX_SB_GPU_L1_DN_C → C3D6 0.1 UF 10% 6.3 V X5R 402 → PEX_SB_GPU_L1_DN OUT 4 62
62 4 IN	PEX_GPU_SB_L0_DP	Y16	PEX_RX0_DP	PEX_TX0_DP	AA17 PEX_SB_GPU_L0_DP_C → C3D3 0.1 UF 10% 6.3 V X5R 402 → PEX_SB_GPU_L0_DP OUT 4 62
62 4 IN	PEX_GPU_SB_L0_DN	AA16	PEX_RX0_DN	PEX_TX0_DN	AB17 PEX_SB_GPU_L0_DN_C → C3D4 0.1 UF 10% 6.3 V X5R 402 → PEX_SB_GPU_L0_DN OUT 4 62
62 IN	KER_DBG_RXD	A3	UART0_RXD<UP>	UART0_TXD	A2 KER_DBG_TXD_R → R2C9 47 OHM 5% CH 402 → KER_DBG_TXD OUT 62
				TST_PT	E18 KSB_DEBUG → 1 DB3P3

GPIO15	F2	AUD_SPI_MISO_R	IN 24 62
GPIO14	F3	AUD_SSB_R	OUT 24 62
GPIO13	E1	SCART_RGB	OUT 37 62
GPIO12	E4	AUD_RST_N	OUT 33
GPIO11	E3	AUD_RDY_BSBY_R	OUT 24 62
GPIO10	F4 62	FAN_TACH_SMM_R	→ R2P9 5% CH 0 OHM 402 → FAN_TACH IN 36 25
GPIO9	G4	WSS_CNTL0	OUT 37 62
GPIO8	G3	WSS_CNTL1	OUT 37 62
GPIO7	D3	AUD_SPI_MOSI_R	OUT 24 62
GPIO6	D4	AUD_SPI_CLK_R	OUT 24 62
GPIO5	E2	SB_GPIO<5>	BI 24 62
GPIO4	C1	SB_GPIO<4>	OUT 24 62
GPIO3	C2	SB_GPIO<3>	OUT 24 62
GPIO2	D1	SB_GPIO<2>	OUT 24 62
GPIO1	B1	SB_GPIO<1>	BI 24 62
GPIO0	B2	SB_GPIO<0>	OUT 24 62

65 IN	SB_TCLK	T19	TCK<DN>
65 OUT	SB_TDO	R19	TDO
65 IN	SB_TDI	R20	TDI<UP>
65 IN	SB_TMS	U19	TMS<UP>
65 IN	SB_TRST	N19	TRST<DN>

FT3T8 FTP 1
FT3T7 FTP 1
FT3T6 FTP 1
FT3T5 FTP 1
FT3T4 FTP 1

V_3P3STBY

R3G19 10 KOHM 5% CH 402
R2C21 0 OHM 5% CH 402
R2C1 10 KOHM 5% EMPTY 402

62 24 IN AUD_SPI_MOSI_R → AUD_SPI_MOSI OUT 35

V_3P3STBY

R3G18 10 KOHM 5% CH 402
R2C25 0 OHM 5% CH 402
R2C24 10 KOHM 5% EMPTY 402

62 24 OUT AUD_SPI_MISO_R → AUD_SPI_MISO IN 35

V_3P3STBY

R3G3 10 KOHM 5% CH 402
R2C23 0 OHM 5% CH 402
R2C22 10 KOHM 5% EMPTY 402

62 24 IN AUD_SPI_CLK_R → AUD_SPI_CLK OUT 35

V_3P3STBY

R2G6 10 KOHM 5% CH 402
R2G5 0 OHM 5% CH 402
R2G7 10 KOHM 5% EMPTY 402

62 24 IN AUD_RDY_BSBY_R → AUD_RDY_BSBY OUT 35

V_3P3STBY

R3G20 10 KOHM 5% CH 402
R2P5 0 OHM 5% CH 402
R2C26 10 KOHM 5% EMPTY 402

62 24 IN AUD_SSB_R → AUD_SSB OUT 35

DEBUG BUS

NET NAME	DEBUG BUS BIT
SB_GPIO<0>	0
SB_GPIO<2>	1
SB_GPIO<3>	2
SB_GPIO<4>	3
AUD_SPI_CLK_R	4
SB_GPIO<5>	5
WSS_CNTL1	6
WSS_CNTL0	7
FAN_TACH	8
AUD_RDY_BSBY_R	9
SCART_RGB	10
AUD_SSB_R	11
AUD_SPI_MISO_R	12

[PAGE_TITLE=KSB, PCIEX + SMM GPIO + JTAG]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	24/74	B	1.0

KSB, SMC

U3D1 KSB IC

5 OF 9

N: DBG_LED0 PULLDOWN = SMC PRODUCTION MODE
DBG_LED0 PULLUP = SMC DEVELOPMENT MODE

SMC_P4_GPIO7 SMC_P4_GPIO6 SMC_P4_GPIO5 SMC_P4_GPIO4 SMC_P4_GPIO3 SMC_P4_GPIO2 SMC_P4_GPIO1 SMC_P4_GPIO0

SMC_P3_GPIO7 SMC_P3_GPIO6 SMC_P3_GPIO5 SMC_P3_GPIO4 SMC_P3_GPIO3 SMC_P3_GPIO2 SMC_P3_GPIO1 SMC_P3_GPIO0

SMC_P2_GPIO7 SMC_P2_GPIO6 SMC_P2_GPIO5 SMC_P2_GPIO4 SMC_P2_GPIO3 SMC_P2_GPIO2 SMC_P2_GPIO1 SMC_P2_GPIO0

SMC_P1_GPIO7 SMC_P1_GPIO6 SMC_P1_GPIO5 SMC_P1_GPIO4 SMC_P1_GPIO3 SMC_P1_GPIO2 SMC_P1_GPIO1 SMC_P1_GPIO0

SMC_P0_GPIO7 SMC_P0_GPIO6 SMC_P0_GPIO5 SMC_P0_GPIO4 SMC_P0_GPIO3 SMC_P0_GPIO2 SMC_P0_GPIO1 SMC_P0_GPIO0

SMC_PWM1 SMC_PWM0

X850744-001 PBGA404

SMC_P1,2,3,4 GPIOS ARE ON V3P3STBY. SMC_P0 GPIOS ARE ON 1P8VSTBY

DEBUG BUS

KSB PIN	DEBUG BUS BIT
SMC_P1_GPIO1	13
FAN_TACH	14
SMC_PWM0	15
SMC_P1_GPIO6	16
SMC_P2_GPIO0	17
SMC_P2_GPIO1	18
SMC_P2_GPIO3	19
SMC_P2_GPIO4	20
SMC_P2_GPIO5	21
SMC_P3_GPIO1	22
SMC_P3_GPIO2	23

[PAGE_TITLE=KSB, SMC]

DRAWING
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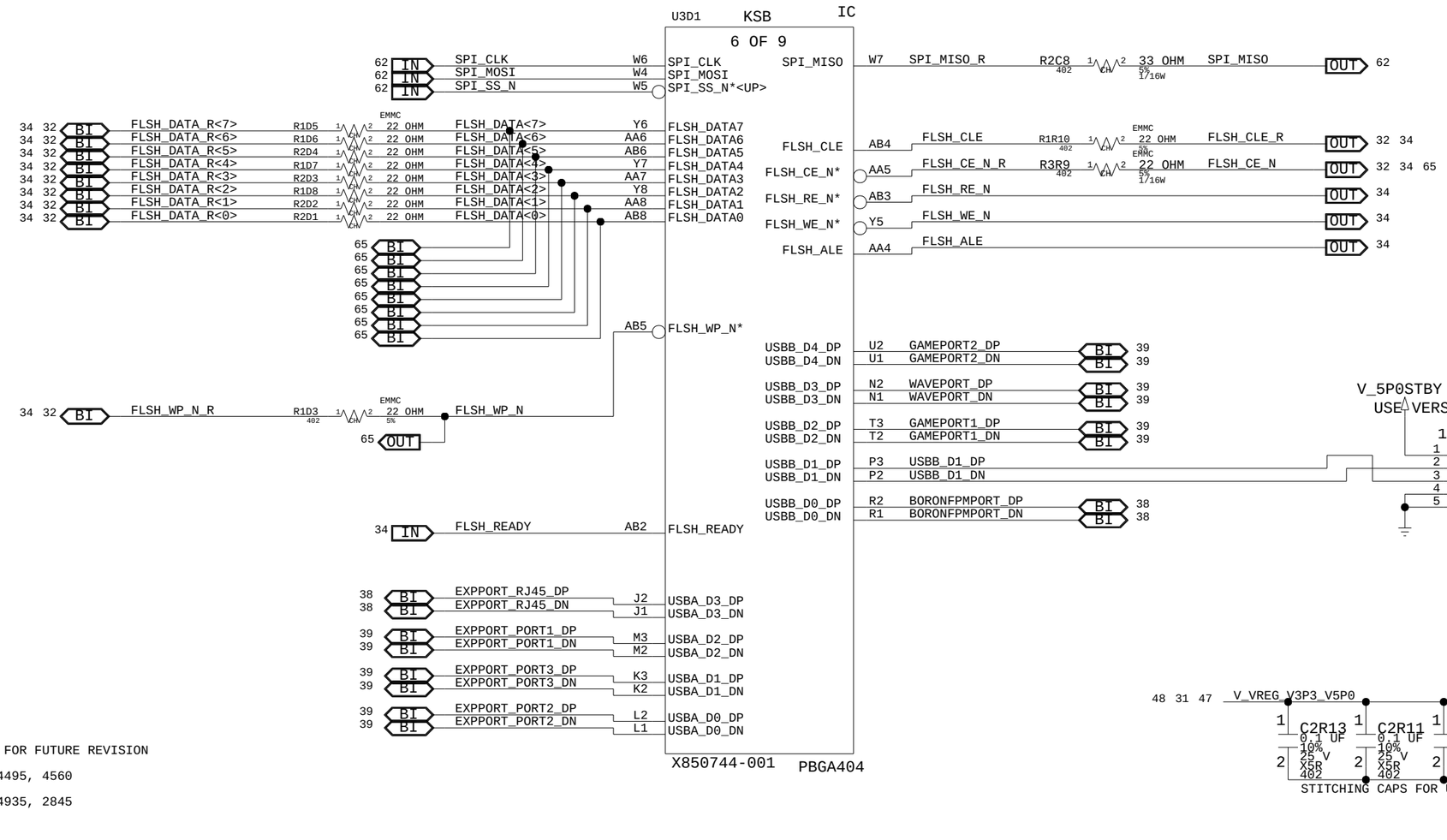
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	25/74	B	1.0

KSB, FLASH + USB + SPI

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R1D5	X800967-001	CH	RES,0OHM,0402	NAND
R1D6	X800967-001	CH	RES,0OHM,0402	NAND
R2D4	X800967-001	CH	RES,0OHM,0402	NAND
R1D7	X800967-001	CH	RES,0OHM,0402	NAND
R2D3	X800967-001	CH	RES,0OHM,0402	NAND
R1D8	X800967-001	CH	RES,0OHM,0402	NAND
R2D2	X800967-001	CH	RES,0OHM,0402	NAND
R2D1	X800967-001	CH	RES,0OHM,0402	NAND
R1D3	X800967-001	CH	RES,0OHM,0402	NAND
R1R10	X800967-001	CH	RES,0OHM,0402	NAND
R3R9	X800451-001	CH	RES,10OHM,0402	NAND

PACK_IGNORE=TRUE



[PAGE_TITLE=KSB, FLASH + USB + SPI]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 26/74	FAB B	REV 1.0

KSB, ETHERNET + AUDIO + SATA

V_3P3STBY

C3P32 0.1 UF 10% 6.3 V X5R 402
C3P35 0.1 UF 10% 6.3 V X5R 402
C3P33 0.1 UF 10% 6.3 V X5R 402
C3P34 0.1 UF 10% 6.3 V X5R 402

V_1P2STBY

STITCHING CAPS FOR I2S SIGNALS,PARTICULARLY MCLK.
PLACE AS CLOSE AS POSSIBLE TO I2S_MCLK, I2S_BCLK, I2S_SD, AND I2S_WS.

U3D1 KSB IC
7 OF 9

38 B1	ENET_RX_DN	H2	MDIN1	MDIN0	G1	ENET_TX_DN	B1 38
38 B1	ENET_RX_DP	H3	MDIP1	MDIP0	G2	ENET_TX_DP	B1 38
			I2S_MCLK_OUT		B18	I2S_MCLK_R	R3P14 47 OHM 402 5% CH I2S_MCLK OUT 33
			I2S_BCLK_OUT		B17	I2S_BCLK_R	R3P10 47 OHM 402 5% CH I2S_BCLK OUT 33
			I2S_SD		A17	I2S_SD_R	R3P9 47 OHM 402 5% CH I2S_SD OUT 33
			I2S_WS		C17	I2S_WS_R	R3P8 47 OHM 402 5% CH I2S_WS OUT 33
41 IN	HDD_RX_DP	Y2	SATA1_RX_DP	SPDIF_OUT	D16	SPDIF_OUT_R	R3P20 0 OHM 402 5% CH SPDIF_OUT OUT 37 39
41 IN	HDD_RX_DN	Y3	SATA1_RX_DN				
41 IN	ODD_RX_DP	V2	SATA0_RX_DP				
41 IN	ODD_RX_DN	V3	SATA0_RX_DN				

R3P12 10 KOHM 5% CH 402
R3P13 10 KOHM 5% CH 402
R3P19 10 KOHM 5% CH 402

SATA1_TX_DP	AA2	HDD_TX_DP	OUT 41
SATA1_TX_DN	AA1	HDD_TX_DN	OUT 41
SATA0_TX_DP	W2	ODD_TX_DP	OUT 41
SATA0_TX_DN	W1	ODD_TX_DN	OUT 41

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[PAGE_TITLE=KSB, ETHERNET + AUDIO + SATA]

DRAWING
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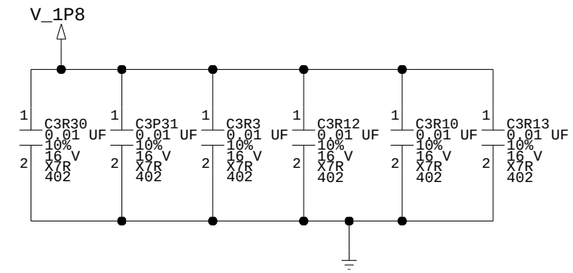
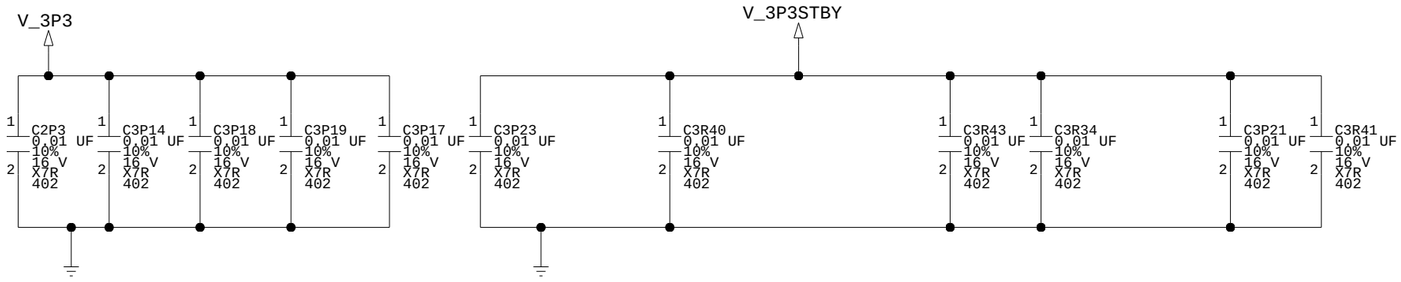
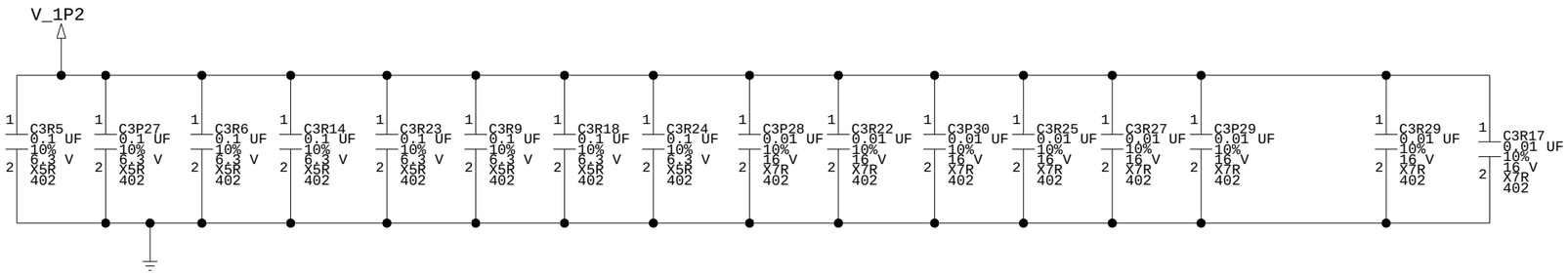
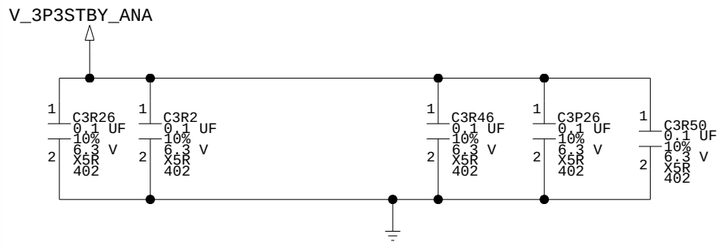
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	27/74	B	1.0

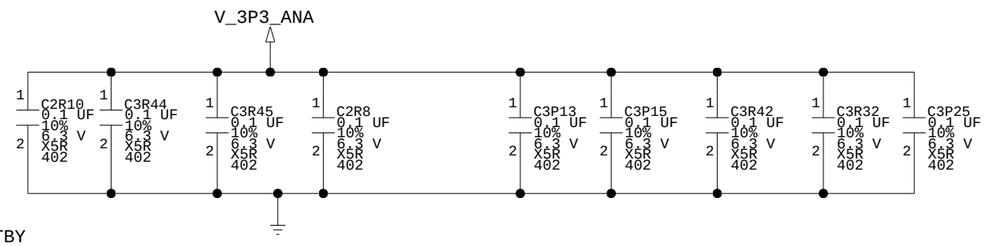
KSB,DECOUPLING

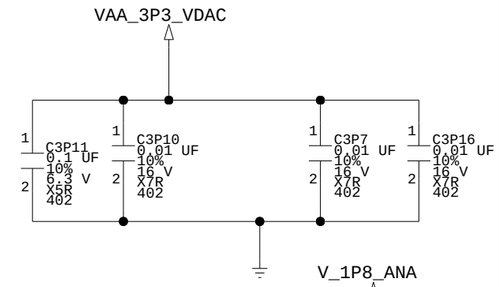


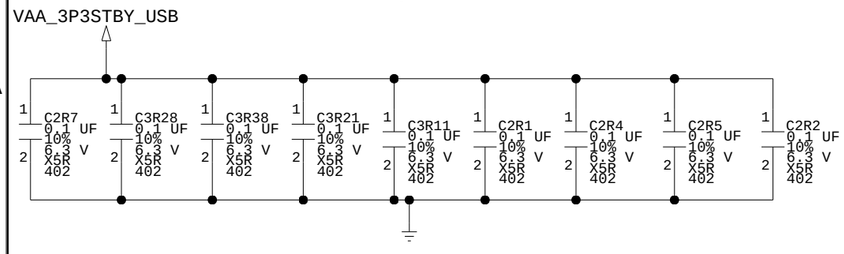


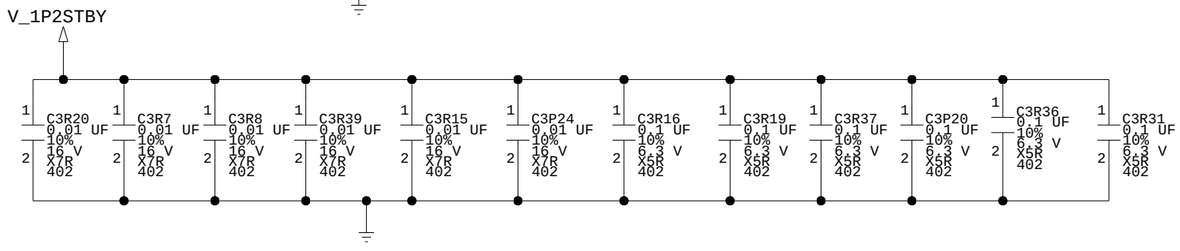


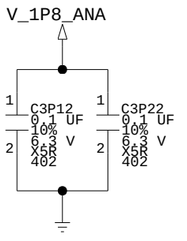










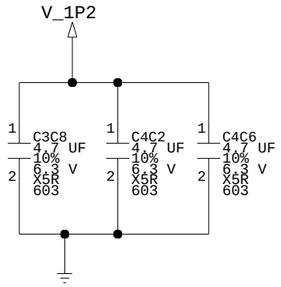


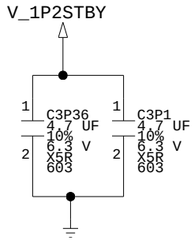
[PAGE_TITLE=KSB, DECOUPLING]

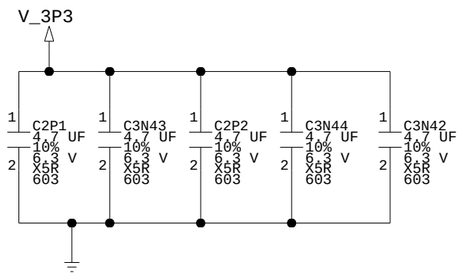
DRAWING
Wed Mar 14 01:47:44 2012

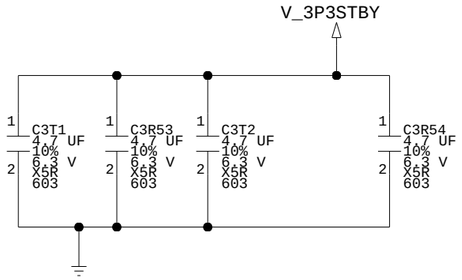
MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 28/74	FAB B	REV 1.0

KSB, BULK DECOUPLING







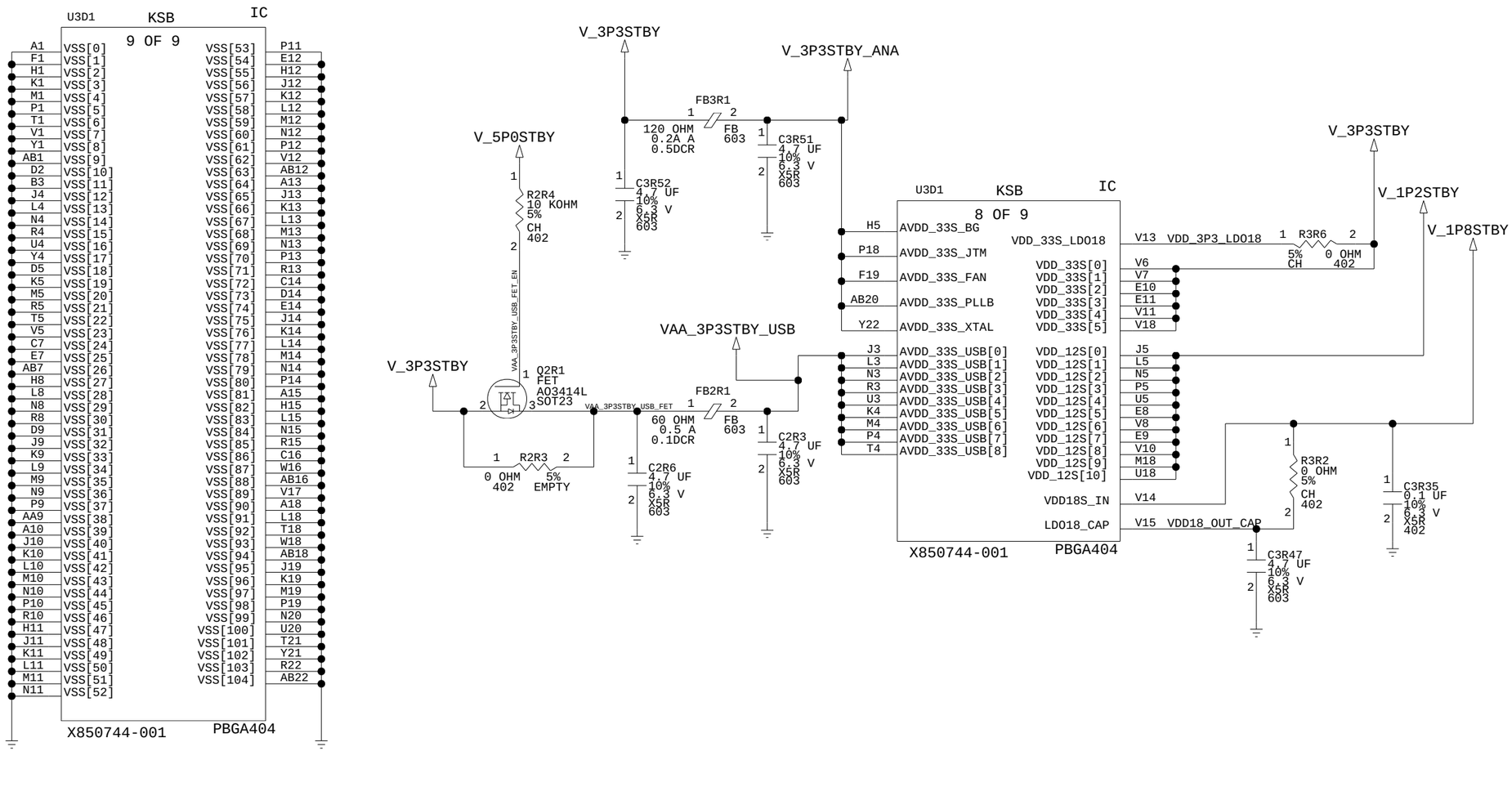


[PAGE_TITLE=KSB, BULK DECOUPLING]

DRAWING
Wed Mar 14 01:47:46 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 29/74	FAB B	REV 1.0

KSB, STANDBY POWER + GROUND

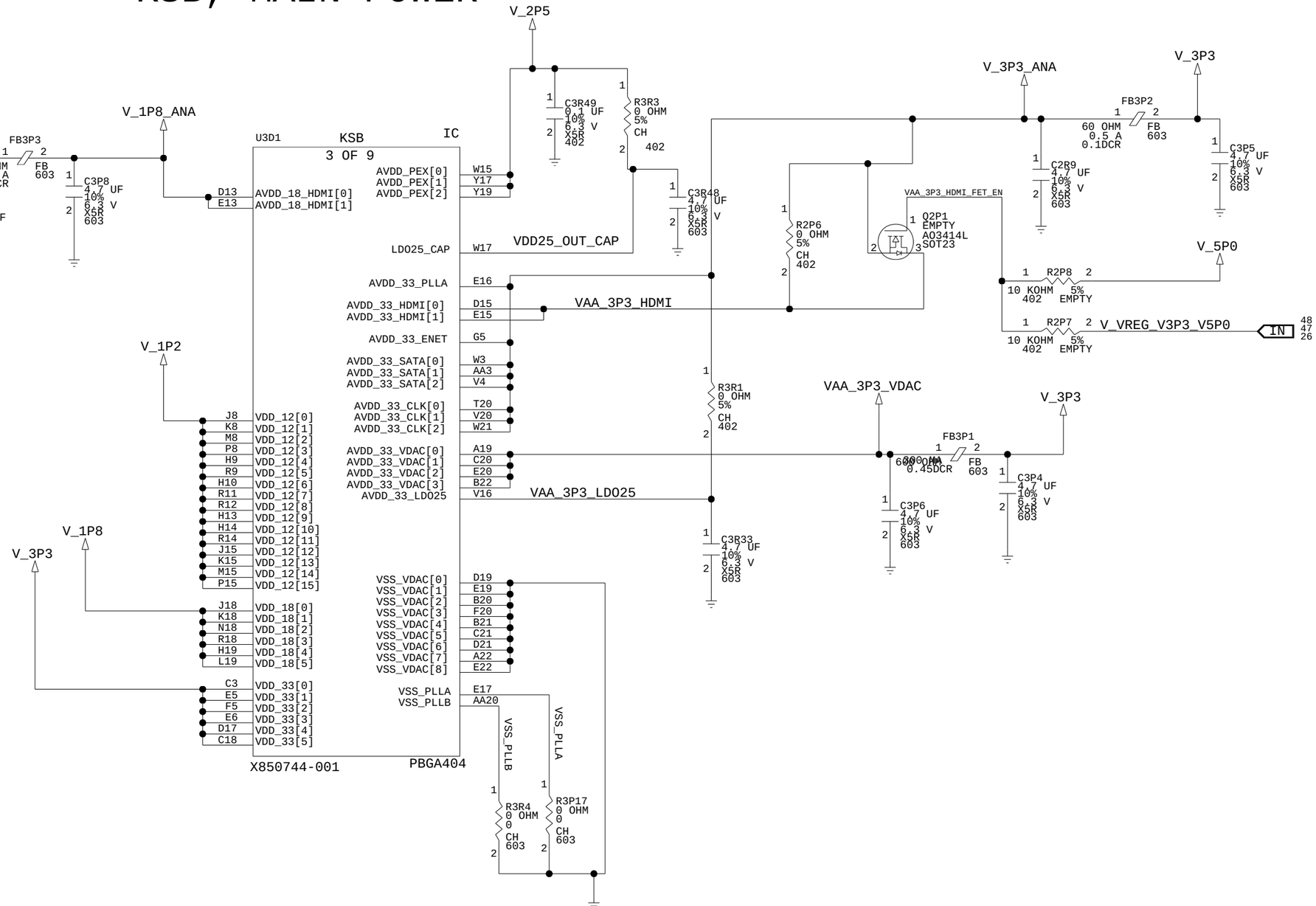


[PAGE_TITLE=KSB, STANDBY POWER]

DRAWING
Wed Mar 14 01:47:31 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	30/74	B	1.0

KSB, MAIN POWER



[PAGE_TITLE=KSB, MAIN POWER]

DRAWING
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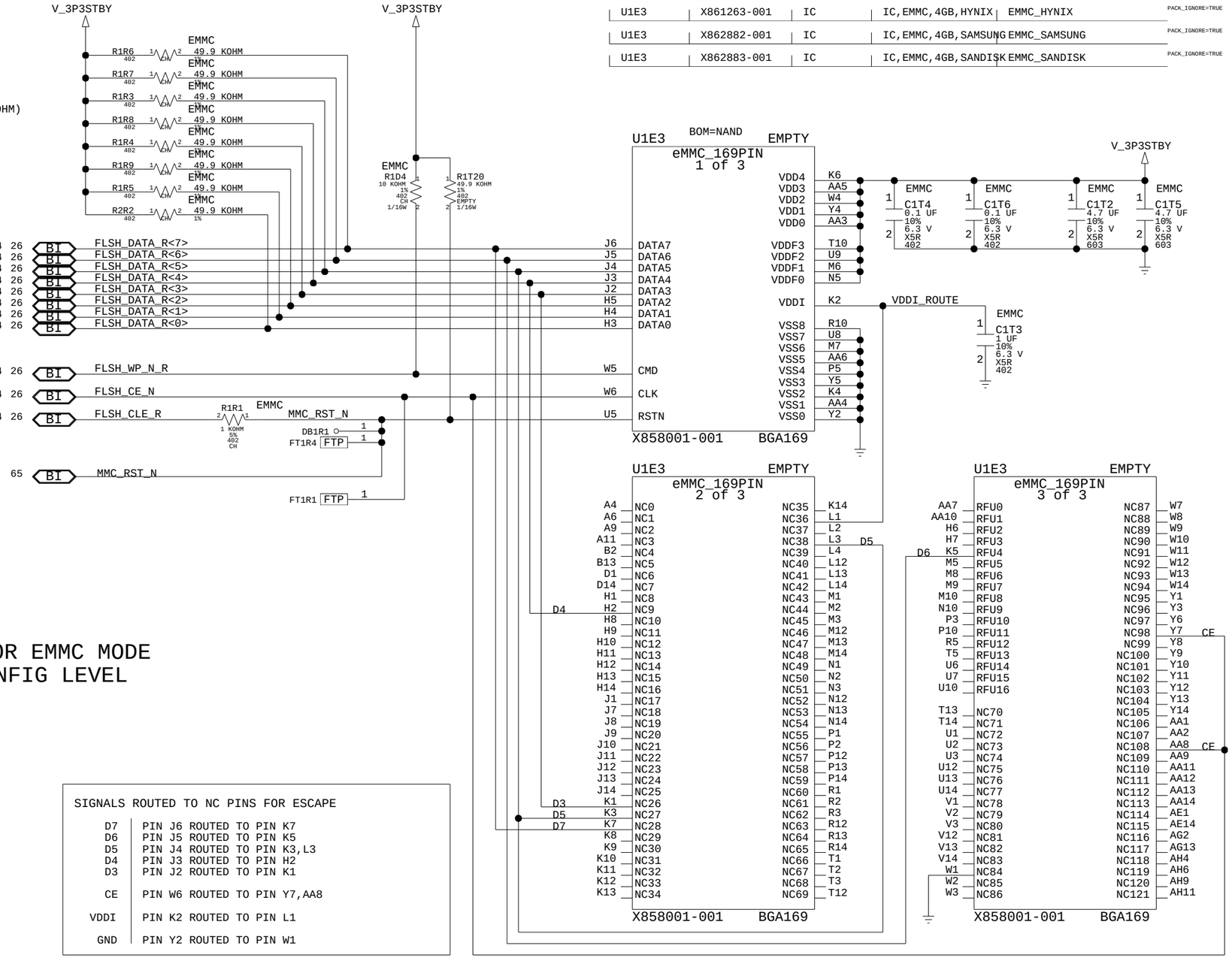
MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 31/74	FAB B	REV 1.0

EMMC

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY	
U1E3	X861263-001	IC	IC,EMMC,4GB,HYNIX	EMMC_HYNIX	PACK_IGNORE=TRUE
U1E3	X862882-001	IC	IC,EMMC,4GB,SAMSUNG	EMMC_SAMSUNG	PACK_IGNORE=TRUE
U1E3	X862883-001	IC	IC,EMMC,4GB,SANDISK	EMMC_SANDISK	PACK_IGNORE=TRUE

TOSHIBA 32NM NEEDED STRONGER PULLUPS (20KOHM)



ALL COMPONENTS ON THIS PAGE ARE FOR EMMC MODE
TO BE STUFFED/UNSTUFFED AT CONFIG LEVEL

SIGNALS ROUTED TO NC PINS FOR ESCAPE	
D7	PIN J6 ROUTED TO PIN K7
D6	PIN J5 ROUTED TO PIN K5
D5	PIN J4 ROUTED TO PIN K3,L3
D4	PIN J3 ROUTED TO PIN H2
D3	PIN J2 ROUTED TO PIN K1
CE	PIN W6 ROUTED TO PIN Y7,AA8
VDDI	PIN K2 ROUTED TO PIN L1
GND	PIN Y2 ROUTED TO PIN W1

[PAGE_TITLE=MMC + FLASH]

DRAWING
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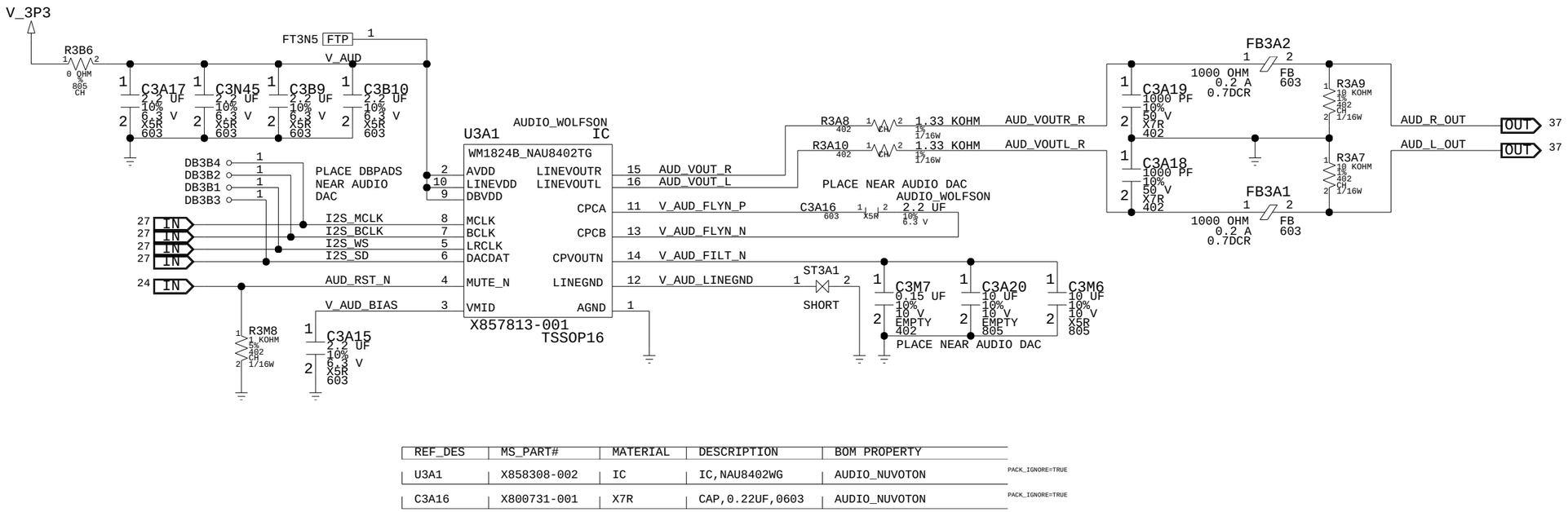
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	32/74	B	1.0

KSB OUT, AUDIO



REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
U3A1	X858308-002	IC	IC,NAU8402WG	AUDIO_NUVOTON PACK_IGNORE=TRUE
C3A16	X800731-001	X7R	CAP,0.22UF,0603	AUDIO_NUVOTON PACK_IGNORE=TRUE

[PAGE_TITLE=PSB OUT, AUDIO]

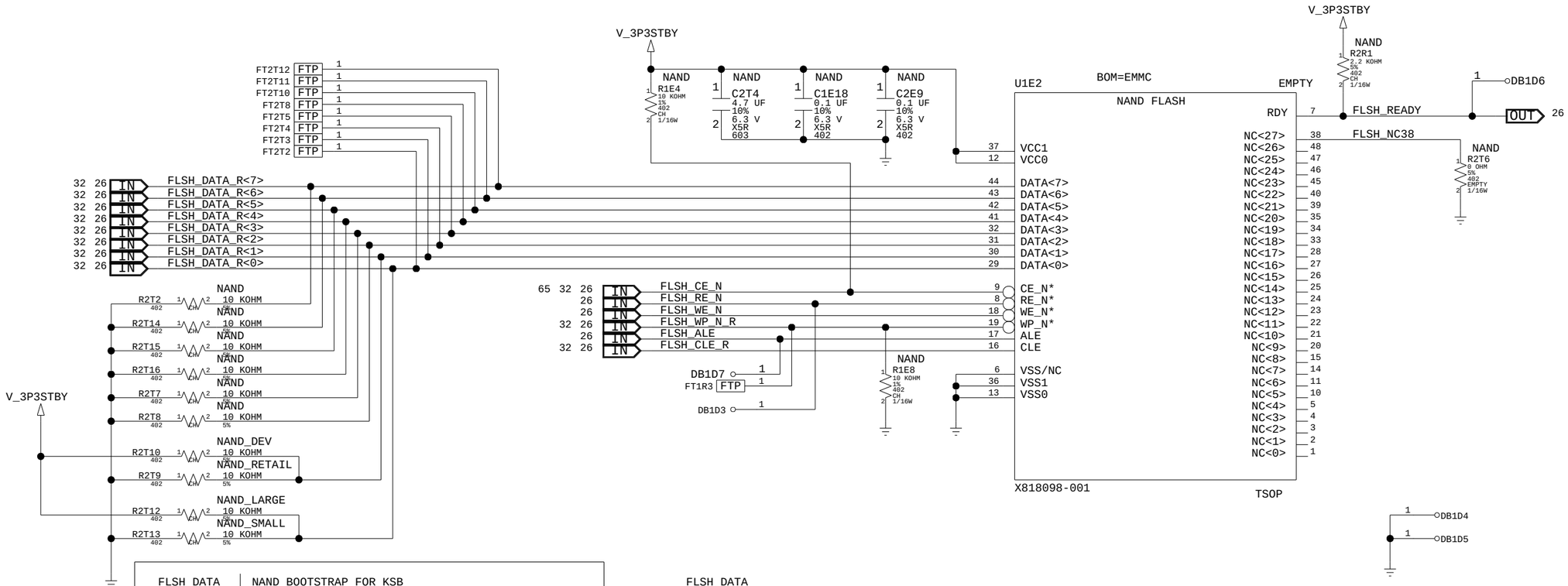
DRAWING
Wed Mar 14 01:47:35 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	33/74	B	1.0

KSB OUT, FLASH

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY	
U1E2	X803471-003	IC	IC,NAND,16MB	NAND_16MB_HYNIX	PACK_IGNORE=TRUE
U1E2	X818098-001	IC	IC,NAND,512MB	NAND_512MB_HYNIX	PACK_IGNORE=TRUE

ALL COMPONENTS ON THIS PAGE ARE FOR NAND MODE
TO BE STUFFED/UNSTUFFED AT CONFIG LEVEL



FLSH_DATA 1	FLSH_DATA 0	NAND BOOTSTRAP FOR KSB FLASH CONFIGURATION	CONFIG
LOW	LOW	0.5KB, 16KB BLOCKS, 128MBIT	RETAIL
LOW	HIGH	0.5KB, 16KB BLOCKS, 512MBIT	RETAIL
HIGH	LOW	2KB PAGES, 128KB BLOCKS, 1/2/4 GBIT	DEV
HIGH	HIGH	4KB PAGES, 256KB BLOCKS, 2/4/8 GBIT	DEV

FLSH_DATA
2 1 0

0 0 0 Raw NAND mode, 0.5kB, 16kB blocks, 128Mb
0 0 1 Raw NAND mode, 0.5kB, 16kB blocks, 512Mb
0 1 0 Raw NAND mode, 2.0kB, 128kB blocks, vary size
0 1 1 Raw NAND mode,
1 0 0 Raw NAND mode, 4.0kB, 256kB blocks, vary size
1 0 1 Raw NAND mode,
1 1 0 Raw NAND mode,
1 1 1 MMC mode

[PAGE_TITLE=PSB OUT, FLASH]

DRAWING
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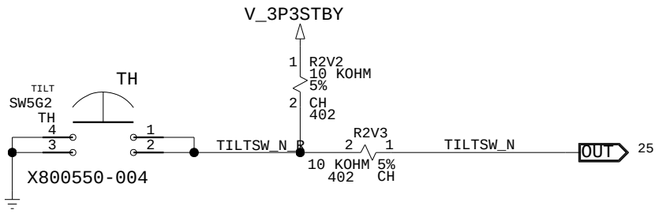
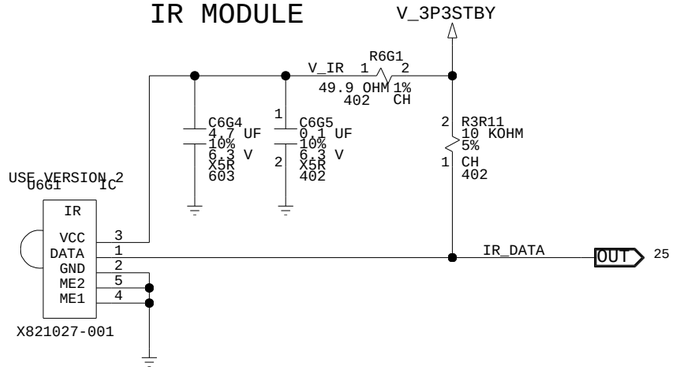
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	34/74	B	1.0

CONN, INFARED + SWITCHES + AUDIBLE F/B

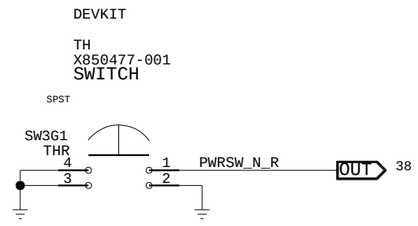
TILT SWITCH, SOLICO



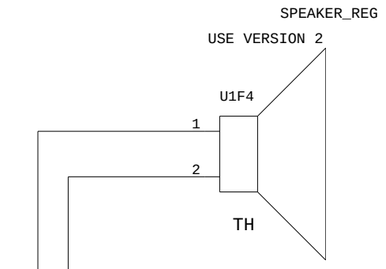
IR MODULE



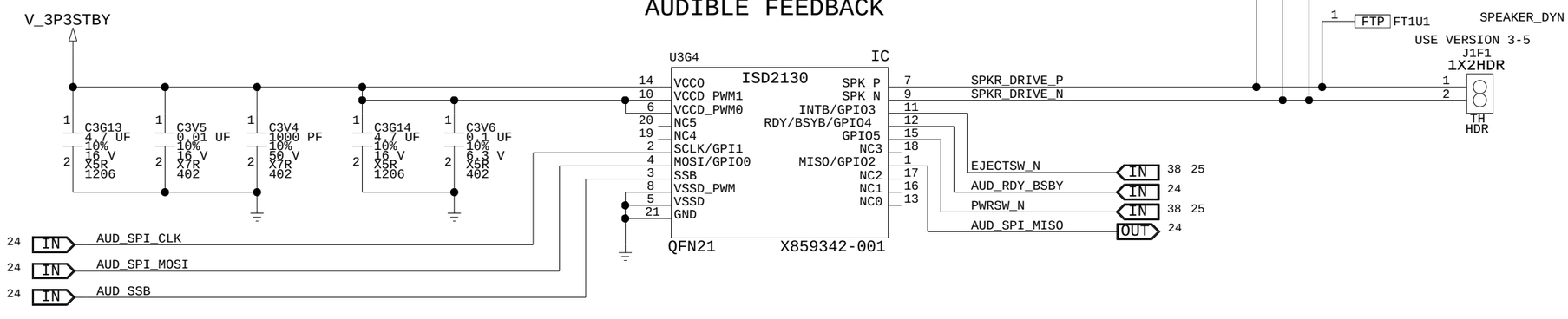
DEVKIT



POWER BUTTON



AUDIBLE FEEDBACK

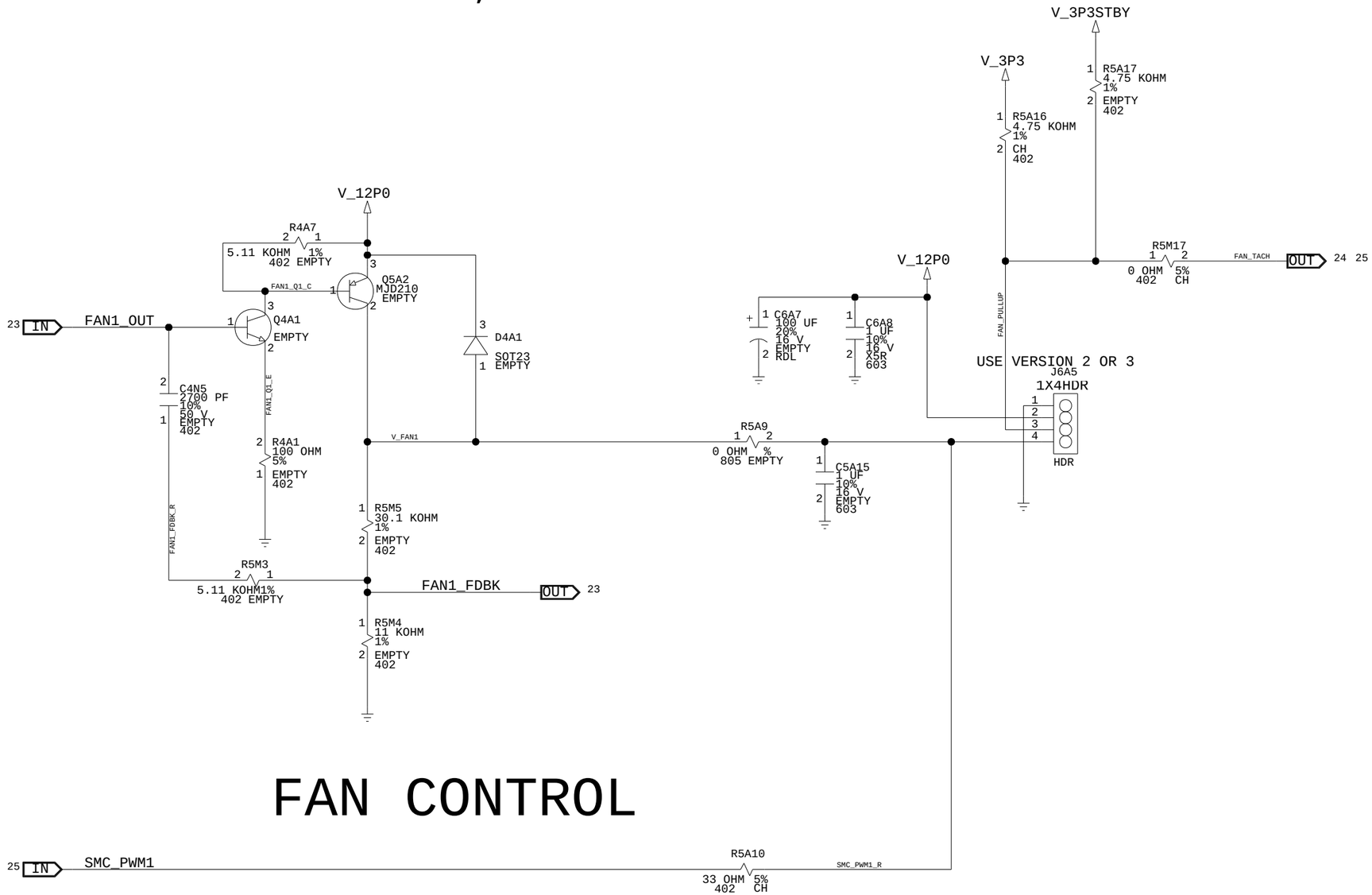


[PAGE_TITLE=CONN,INFRARED+SWITCHES+AUDIBLE F/B]

DRAWING
Wed Mar 14 01:47:53 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	35/74	B	1.0

CONN, FAN



FAN CONTROL

CONN, AVIP

DAC	STANDARD	ADVANCED	SDTV	HDTV	SCART	VGA
A	N/A	Y(LUMA)	Y	Y	G	G
B	N/A	C(CHROMA)	PR	PR	R	R
C	N/A	N/A	PB	PB	B	B
D	CVBS(COMP)	CVBS(COMP)	CVBS	N/A	CVBS	CVBS

V_5P0 — RT3A1 01.10 A THRMSTR 1206 — C2A8 4.7 UF 10% 6.3 V X5R 603 — C3A12 470 PF 5% 50 V X7R 402 — V_AVIP OUT 39 40

DBPAD ON SPDIF TO BE PLACED AS CLOSE TO CONN AS POSSIBLE

USE VERSION 2 — C3A13 22 PF 5% 50 V NPO 402 — EG3A6 X807267-002 — DIO 402

J4A2 CONN — XENON AVIP CONNECTOR — X856166-001 TH

29	V_AVIP		
27	V_AVIP_RET		
37 IN	VID_DACA_OUT	4	VID_DACA_OUT
		2	VID_DACA_RET
37 IN	VID_DACB_OUT	3	VID_DACB_OUT
		1	VID_DACB_RET
37 IN	VID_DACC_OUT	8	VID_DACC_OUT
		6	VID_DACC_RET
37 IN	VID_DACD_OUT	7	VID_DACD_OUT
		5	VID_DACD_RET
37 IN	VID_HSYNC_OUT	11	VID_HSYNC_OUT
		9	VID_HSYNC_RET
37 IN	VID_VSYNC_OUT	12	VID_VSYNC_OUT
		10	VID_VSYNC_RET
	SPDIF_OUT (DB3A1 1)	25	SPDIF
33 IN	AUD_R_OUT	15	AUD_R_OUT
		13	AUD_R_RET
33 IN	AUD_L_OUT	16	AUD_L_OUT
		14	AUD_L_RET
	WSS_CNTL_OUT_R	17	WSS_CNTL
	SCART_RGB_OUT	19	SCART_RGB
EXT_PWR_ON	30	EXT_PWR_ON_N	OUT 62 65 25 37 66
DDC_CLK	21	HDMI_DDC_CLK	BI 23 40 55
DDC_DATA	23	HDMI_DDC_DATA	BI 23 40 55
AV_MODE2	28	AV_MODE2	OUT 25 37
AV_MODE1	24	AV_MODE1	OUT 25 37
AV_MODE0	20	AV_MODE0	OUT 25 37
GND<2>	26		
GND<1>	22		
GND<0>	18		
SHIELD<3>	34		
SHIELD<2>	33		
SHIELD<1>	32		
SHIELD<0>	31		
MTGB<8-1>			
MTGA<8-1>			

V_3P3STBY

66 25 65 62 37 IN EXT_PWR_ON_N — R3P5 10 KOHM 5% CH 402 — R2N1 10 KOHM 5% CH 402 — R3N6 10 KOHM 5% CH 402 — R2C3 10 KOHM 5% CH 402

25 37 IN AV_MODE2

25 37 IN AV_MODE1

25 37 IN AV_MODE0

C3A2 470 PF 5% 50 V X7R 402 — C2M2 470 PF 5% 50 V X7R 402 — C2M1 470 PF 5% 50 V X7R 402 — C2C2 470 PF 5% 50 V X7R 402

LAYOUT:PLACE CLOSE TO CONNECTOR EMI CAPS

V_12P0 — R3A5 1.82 KOHM 1% CH 402

24 62 IN WSS_CNTL1 — R3A3 5.36 KOHM 1% CH 402

24 62 IN WSS_CNTL0 — R3A4 4.75 KOHM 1% CH 402

Q3A1 XSTR — WSS_CNTL_B — WSS_CNTL_E

R3A6 301 OHM 1% CH 603 — R3A1 10 KOHM 1% CH 402

WSS_CNTL_OUT_R — R3A2 1 KOHM 5% CH 402 — WSS_CNTL_OUT

C3A1 75 PF 5% 50 V NPO 402

V_3P3

24 62 IN SCART_RGB — R2M2 10 KOHM 5% CH 402 — SCART_RGB_R — Q3M1 XSTR — SCART_RGB_OUT_R — R3M7 33 OHM 5% CH 402 — SCART_RGB_OUT

R3M2 10 KOHM 5% CH 402

C3M1 0.01 UF 10% 16 V X7R 402

23 IN VID_VSYNC_OUT_R — R3C25 49.9 OHM 1% CH 402 — VID_VSYNC_OUT OUT 37

USE VERSION 2 — EG4A9 X807267-002 — DIO 402

23 IN VID_HSYNC_OUT_R — R3C24 49.9 OHM 1% CH 402 — VID_HSYNC_OUT OUT 37

USE VERSION 2 — EG4A10 X807267-002 — DIO 402

23 IN VID_DACA_DP — R4A11 4.75 OHM 1% CH 402 — VID_DACA_DP_L — L4A4 .27 UH 0.45 A .360DCR IND 1210 — VID_DACA_OUT OUT 37

USE VERSION 2 — R4A5 75 OHM 1% CH 402 — EG4A8 X807267-002 — DIO 402

V_1P2 — U4M1 — DIO — C4A10 62 PF 5% 50 V NPO 402

V_1P2 — U4A2 — DIO — C4A3 33 PF 5% 50 V NPO 402

23 IN VID_DACC_DP — R4A12 4.75 OHM 1% CH 402 — VID_DACC_DP_L — L4A2 .27 UH 0.45 A .360DCR IND 1210 — VID_DACC_OUT OUT 37

USE VERSION 2 — R4A3 75 OHM 1% CH 402 — EG4A6 X807267-002 — DIO 402

V_1P2 — U4M1 — DIO — C4A8 62 PF 5% 50 V NPO 402

V_1P2 — U4A2 — DIO — C4A5 33 PF 5% 50 V NPO 402

23 IN VID_DACB_DP — R4A10 4.75 OHM 1% CH 402 — VID_DACB_DP_L — L4A3 .27 UH 0.45 A .360DCR IND 1210 — VID_DACB_OUT OUT 37

USE VERSION 2 — R4A4 75 OHM 1% CH 402 — EG4A7 X807267-002 — DIO 402

V_1P2 — U4M2 — DIO — C4A9 62 PF 5% 50 V NPO 402

V_1P2 — U4A1 — DIO — C4A6 33 PF 5% 50 V NPO 402

V_1P2 — C4M3 0.1 UF 10% 25 V X5R 402 — C4M2 0.1 UF 10% 25 V X5R 402

DECOUPLING FOR BAV99DW

23 IN VID_DACD_DP — R4A9 4.75 OHM 1% CH 402 — VID_DACD_DP_L — L4A1 .27 UH 0.45 A .360DCR IND 1210 — VID_DACD_OUT OUT 37

USE VERSION 2 — R4A2 75 OHM 1% CH 402 — EG4A5 X807267-002 — DIO 402

V_1P2 — U4M2 — DIO — C4A7 62 PF 5% 50 V NPO 402

V_1P2 — U4A1 — DIO — C4A4 33 PF 5% 50 V NPO 402

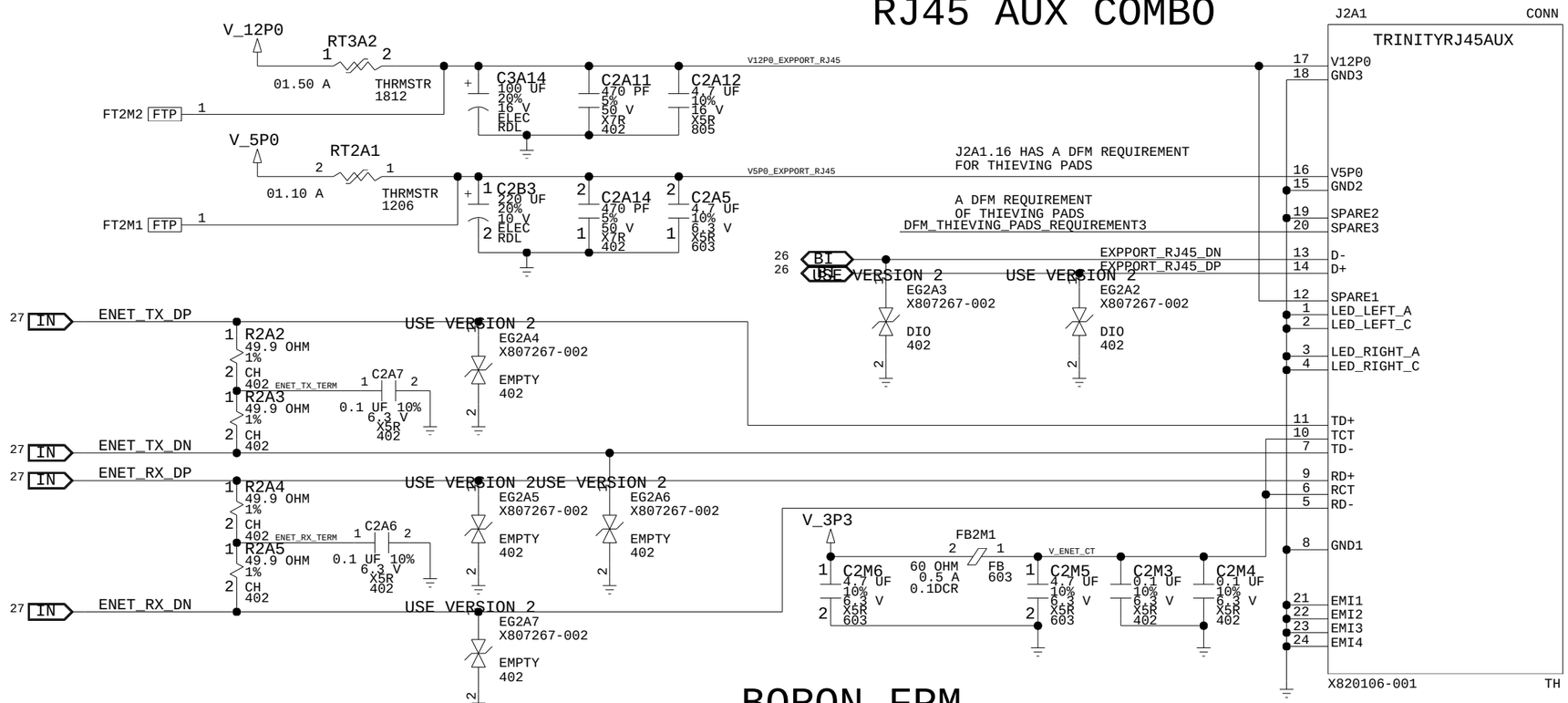
[PAGE_TITLE=[CONN, AVIP]

DRAWING Wed Mar 14 01:47:55 2012

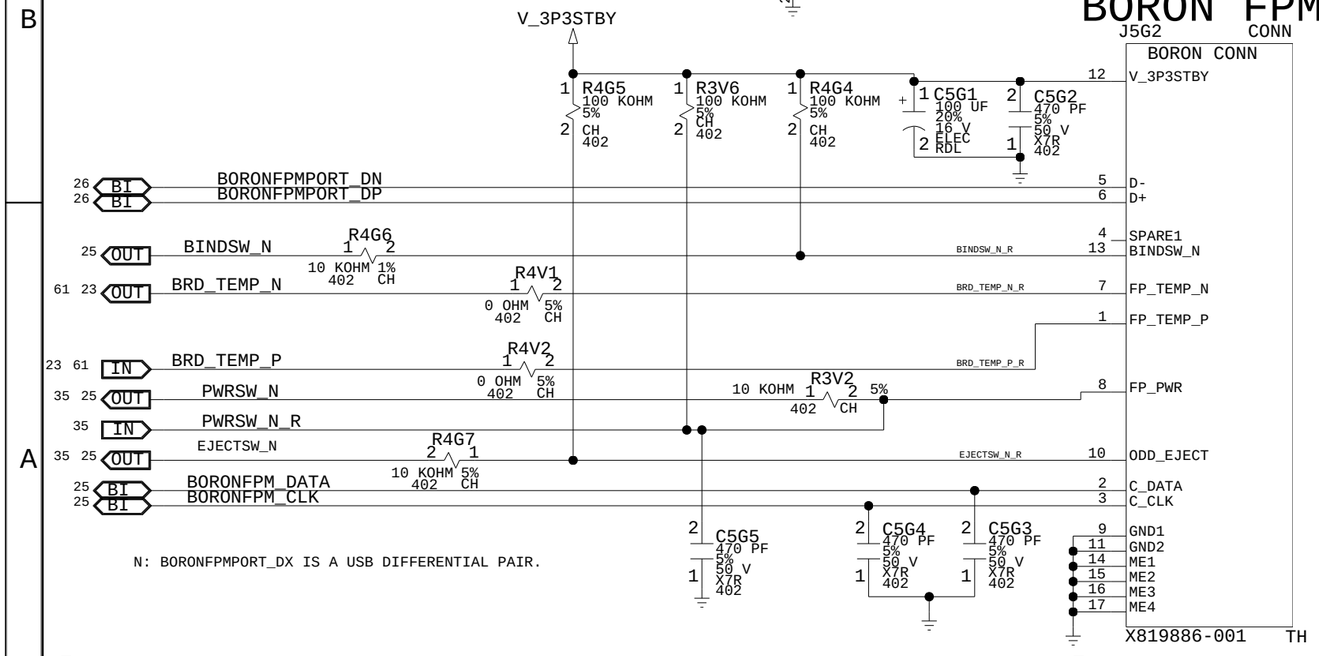
MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 37/74	FAB B	REV 1.0

CONN, RJ45 USB AUX COMBO + BORON + PWR

RJ45 AUX COMBO

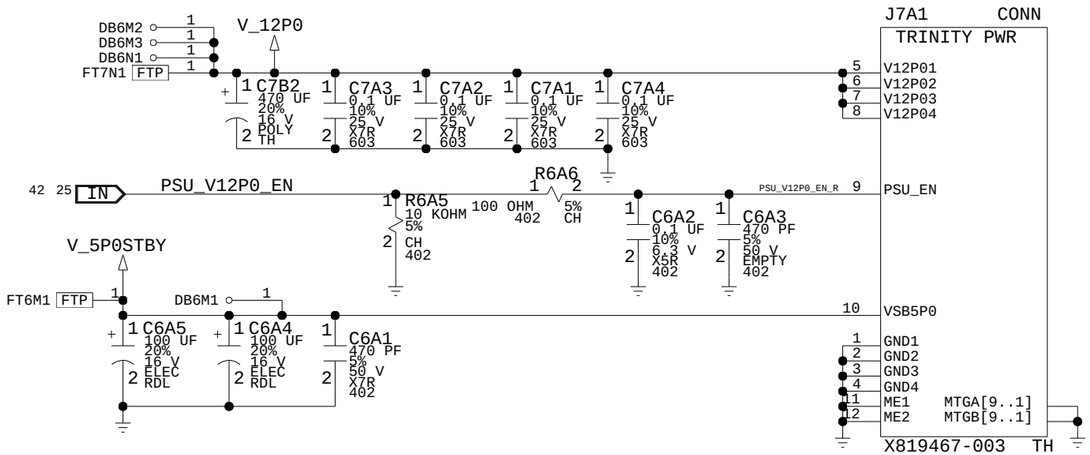


BORON FPM



N: BORONFPMPORT_DX IS A USB DIFFERENTIAL PAIR.

POWER



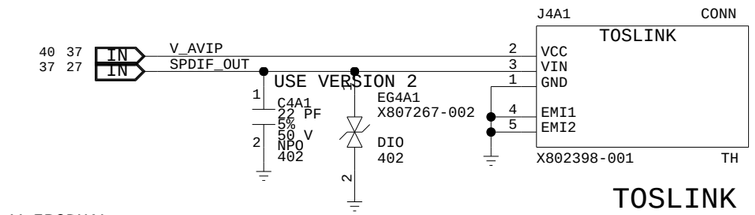
[PAGE_TITLE=CONN, RJ45 AUX COMBO + BORON + PWR]

DRAWING
Wed Mar 14 01:47:56 2012

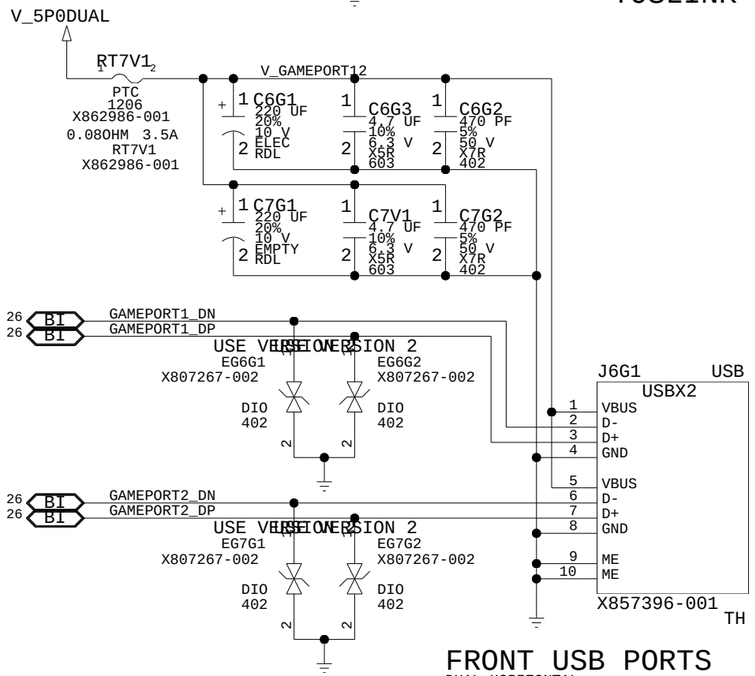
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	38/74	B	1.0

CONN, USB + MEM PORTS + TOSLINK + WAVEPORT

N: ALL DIFFERENTIAL PAIRS ON THIS PAGE ARE USB DIFFERENTIAL PAIRS.

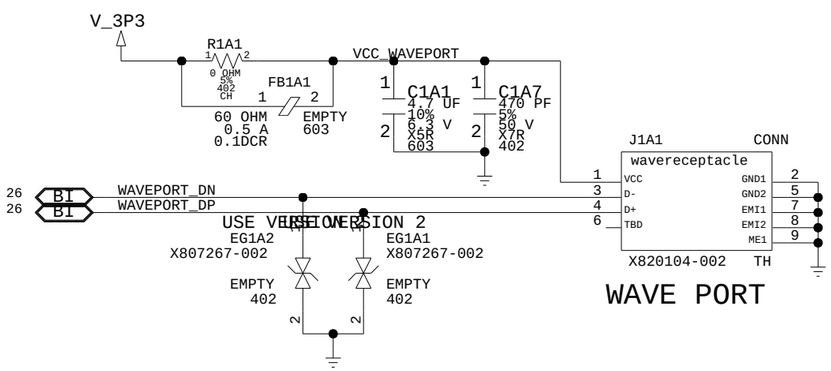


TOSLINK

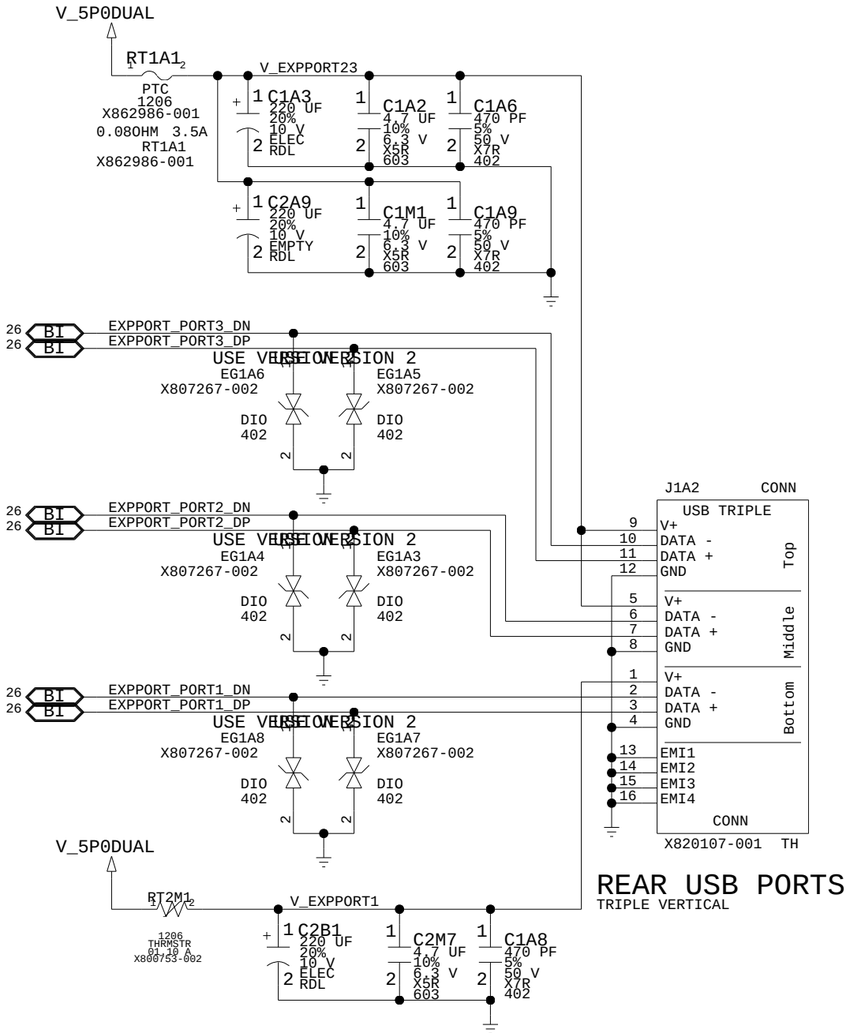


FRONT USB PORTS

DUAL HORIZONTAL



WAVE PORT



REAR USB PORTS

TRIPLE VERTICAL

[PAGE_TITLE=CONN, MEMORY PORTS + GAME PORTS]

DRAWING
Wed Mar 14 01:47:56 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	39/74	B	1.0

CONN, HDMI

FT3M7 FTP 1
FT3M1 FTP 1
23 IN HDMI_TX2_DP
23 IN HDMI_TX2_DN
USE VERSION 2 — EG3A2 X807267-002 — DIO 402
USE VERSION 2 — EG3A1 X807267-002 — DIO 402
FT3M2 FTP 1
FT3M8 FTP 1

FT3M9 FTP 1
FT3M3 FTP 1
23 IN HDMI_TX1_DP
23 IN HDMI_TX1_DN
USE VERSION 2 — EG3A4 X807267-002 — DIO 402
USE VERSION 2 — EG3A3 X807267-002 — DIO 402
FT3M4 FTP 1
FT3M10 FTP 1

FT3M11 FTP 1
FT3M5 FTP 1
23 IN HDMI_TX0_DP
23 IN HDMI_TX0_DN
USE VERSION 2 — EG4A2 X807267-002 — DIO 402
USE VERSION 2 — EG3A5 X807267-002 — DIO 402
FT4M2 FTP 1
FT4M7 FTP 1

FT4M8 FTP 1
FT4M3 FTP 1
23 IN HDMI_TXC_DP
23 IN HDMI_TXC_DN
USE VERSION 2 — EG4A4 X807267-002 — DIO 402
USE VERSION 2 — EG4A3 X807267-002 — DIO 402
FT4M4 FTP 1
FT4M9 FTP 1

V_5P0STBY
R4M2 2 KOHM 1% 2 CH 402
R4M1 2 KOHM 1% 2 CH 402
FT4M5 FTP 1
55 37 23 IN HDMI_DDC_CLK
55 37 23 BI HDMI_DDC_DATA
USE VERSION 2 — EG4M2 X807267-002 — DIO 402
USE VERSION 2 — EG4M1 X807267-002 — DIO 402
FT4M1 FTP 1

39 37 IN V_AVIP
C3A11 0.1 UF 10% 6.3 V X5R 402

J3A1 USE VERSION 3or4 HDR
HDMI
1 TMDS_DATA2_DP
2 TMDS_DATA2_SHD
3 TMDS_DATA2_DN
4 TMDS_DATA1_DP
5 TMDS_DATA1_SHD
6 TMDS_DATA1_DN
7 TMDS_DATA0_DP
8 TMDS_DATA0_SHD
9 TMDS_DATA0_DN
10 TMDS_CLK_DP
11 TMDS_CLK_SHD
12 TMDS_CLK_DN
13 CEC
14 RESERVED
15 SCL
16 SDA
17 DDC_CEC_GND
18 5VCC
19 HOT_PLUG_DET
23 ME4
22 ME3
21 ME2
20 ME1
X806395-002

DB3M1 1 HDMI_CEC

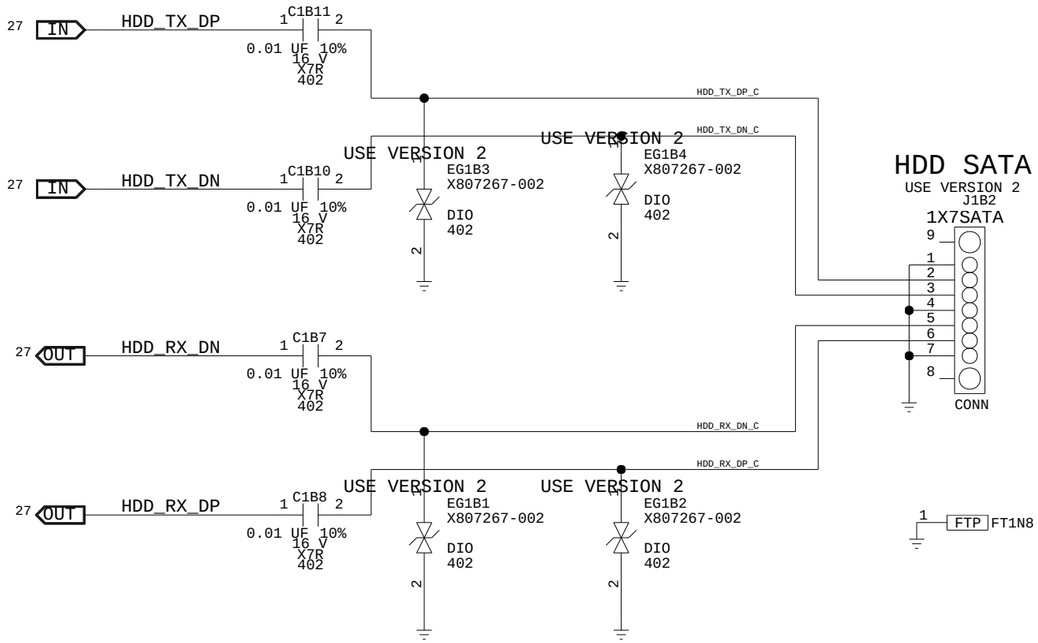
HDMI_HPD_PIN
R4M6 10 KOHM 5% 402 CH
FT4M6 FTP 1
HDMI_HPD OUT 23
USE VERSION 2
R4M5 47.5 KOHM 1% 2 CH 402
EG4M5 X807267-002 — DIO 402

[PAGE_TITLE=CONN, HDMI]

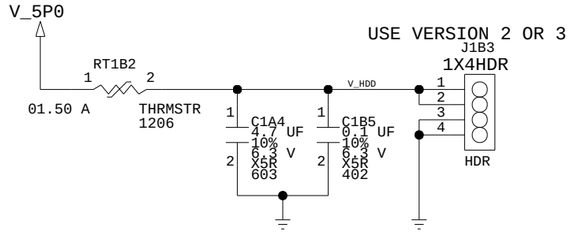
DRAWING
Wed Mar 14 01:47:57 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 40/74	FAB B	REV 1.0

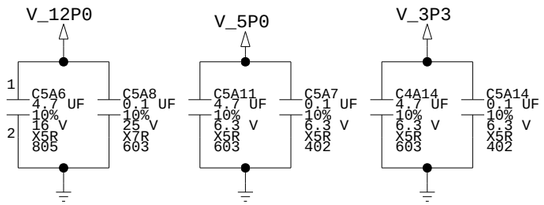
CONN, ODD + HDD



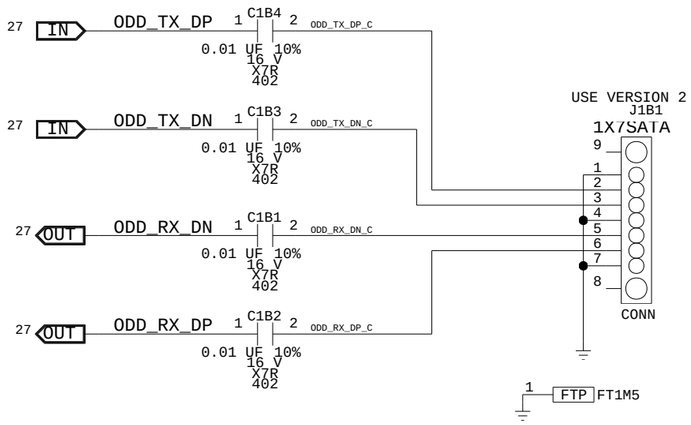
HDD POWER



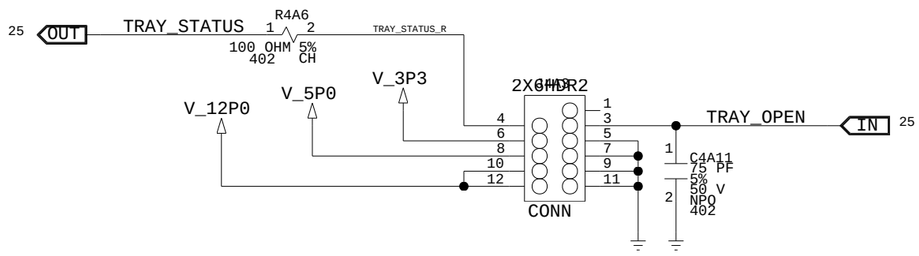
ODD POWER DECOUPLING



ODD SATA



ODD POWER AND CONTROL

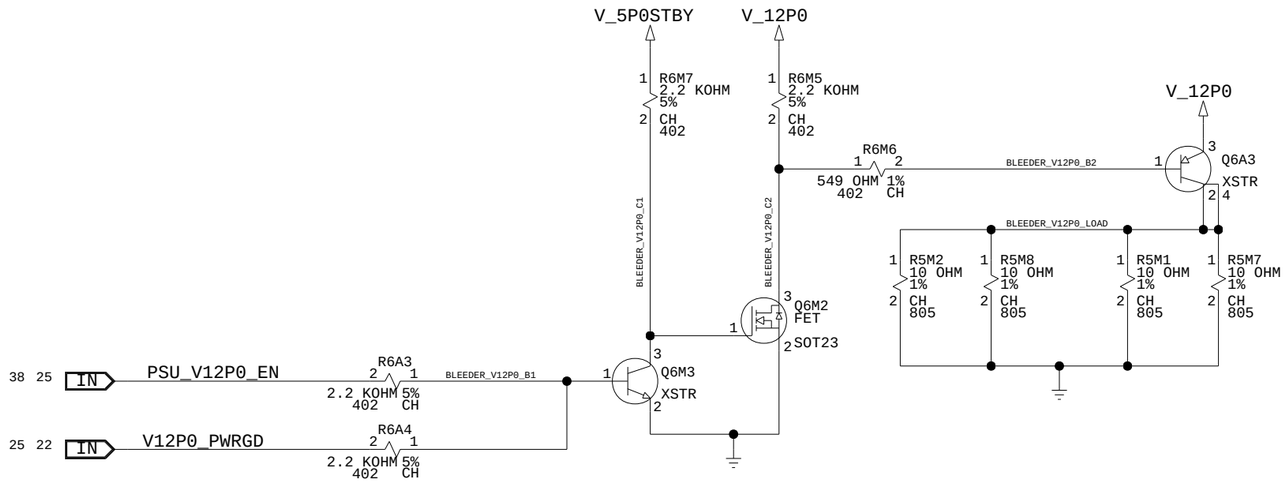


[PAGE_TITLE=CONN, ODD + HDD + MU]

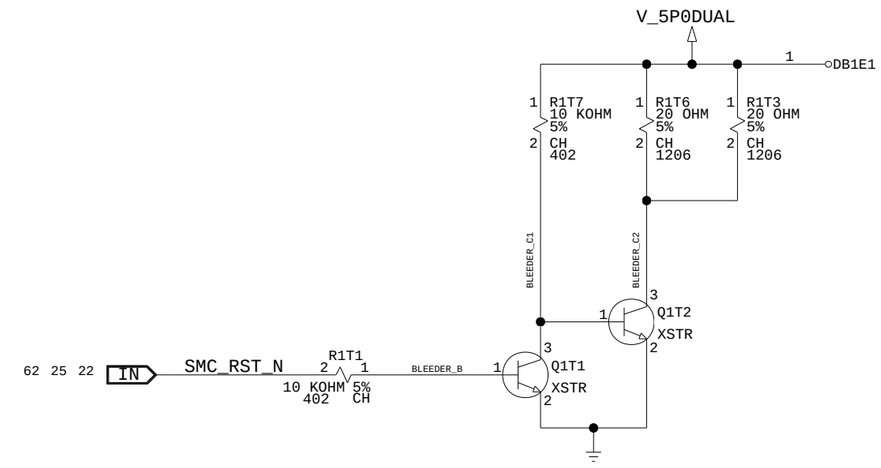
DRAWING
Wed Mar 14 01:47:57 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	41/74	B	1.0

VREG, BLEEDERS



V_12P0 & V_5P0 BLEEDERS



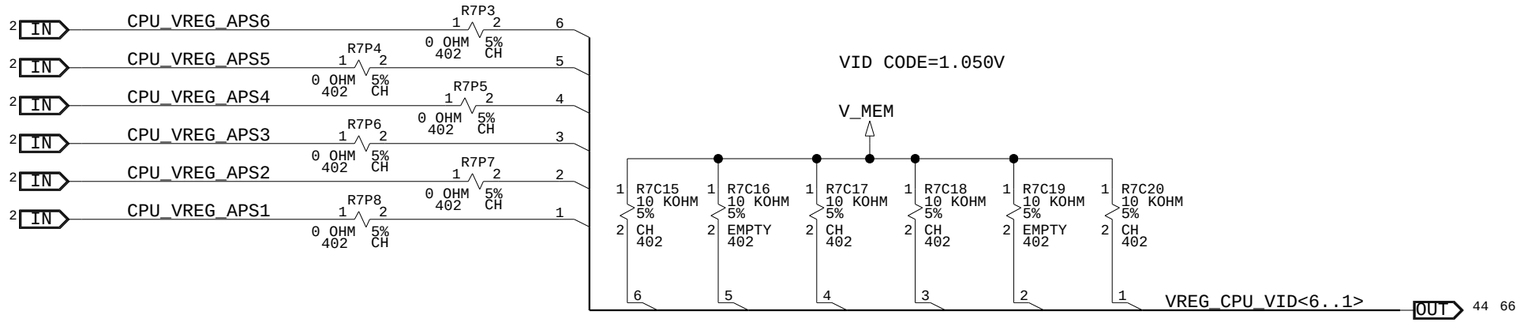
V_5P0DUAL BLEEDER

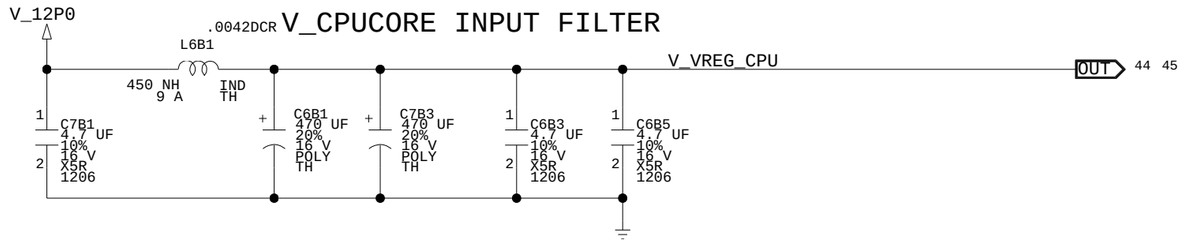
[PAGE_TITLE= VREGS,_BLEEDERS]

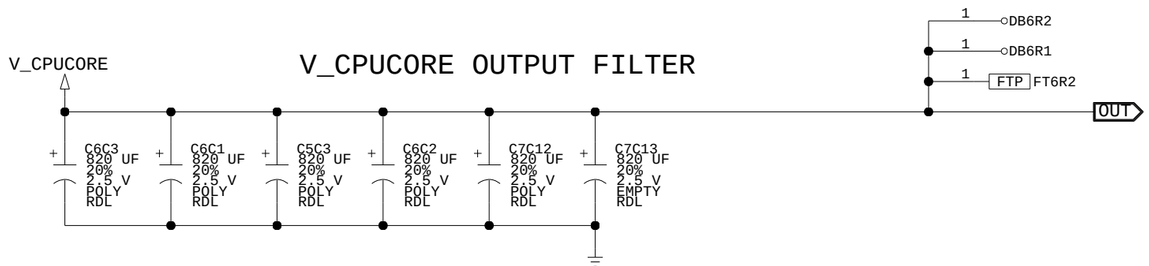
DRAWING
Wed Mar 14 01:47:57 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	42/74	B	1.0

VREGS, INPUT + OUTPUT FILTERS







[PAGE_TITLE=VREGS, INPUT + OUTPUT FILTERS]

DRAWING
Wed Mar 14 01:47:58 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	43/74	B	1.0

VREGS, CPU CONTROLLER

45 43 IN V_VREG_CPU
R7C26 603 681 OHM 1% 1/16W CH
R7C25 603 681 OHM 1% 1/16W CH
R7B5 402 1 KOHM 5% 1/16W CH
VREG_CPU_VCC
VREG_CPU_RAMPADJ_R
R7C22 422 KOHM 1% 402 CH
C7C23 4.7 UF 10% 16 V X5R 1206
C7C22 1 UF 10% 16 V X5R 603
C7P2 0.1 UF 10% 25 V X7R 603
RRAMP
FT3P8 FTP 1
25 IN VREG_CPU_EN
R7C31 10 KOHM 5% 402 CH 1/16W
66 60 59 58 57 56 55 IN PMBUS_CLK
66 60 59 58 57 56 55 BI PMBUS_DATA
45 IN VREG_CPU_PHASE2
R7C23 402 0 OHM 5% 1/16W CH
45 IN VREG_CPU_PHASE1
R7C24 402 0 OHM 5% 1/16W CH
66 OUT VREG_CPU_CSCOMP
R7B1 35.7 KOHM 1% 402 CH 1/16W
RT6C1 603 THRMSTR X801015-001
RCS1
RTH1 TEMP SENSOR
R7C21 6.81 KOHM 1% 402 CH 1/16W
VREG_CPU_CSCOMP_R
R7B3 27.4 KOHM 1% 402 CH 1/16W
RPH2
R7B4 27.4 KOHM 1% 402 CH 1/16W
RPH1
R7B2 52.3 KOHM 1% 402 CH 1/16W
RCS2
C7C15 3300 PF 10% 50 V X7R 402
CCS2
C7C14 3300 PF 10% 50 V X7R 402
CCS1
66 OUT VREG_CPU_CSSUM
66 OUT VREG_CPU_CSREF
V_CPUCORE
ST6B3 SHORT OFFGRID
PLACE SHORT NEXT TO OUTPUT OF DUAL INDUCTOR
C7P1 1000 PF 10% 50 V X7R 402
ST6D1 SHORT OFFGRID
PLACE SHORT NEXT TO POINT OF LOAD
DB7C1
VREG_V_CPUCORE_S
VENABLE
R7C32 0 OHM 5% 805 EMPTY
C7C16 470 PF 5% 402 X7R 50 V CB
VREG_CPU_FB
C7C17 10 PF 5% 402 NPO 50 V CFB
R7P9 1.1 KOHM 1% 402 CH RB
C7C18 1500 PF 10% 402 X7R 50 V CA
VREG_CPU_COMP_R
R7P10 18.2 KOHM 1% 402 CH RA
DB7C2
ST6D2 SHORT OFFGRID
PLACE SHORT NEXT TO POINT OF LOAD

VREG_CPU_VCC3_3P3
C7C20 0.1 UF 10% 6.3 V X5R 402
U7C1 IC NCP4202 X857741-001 QFN29

VREG_CPU_VCC	21	VCC			
VREG_CPU_RAMPADJ	8	RAMPADJ	PWRGD	28	VREG_CPUCORE_PWRGD OUT 25
VREG_CPU_EN	4	EN	IPD VID6	22	VREG_CPU_VID<6> IN 43 66
PMBUS_CLK	3	SCL	IPD VID5	23	VREG_CPU_VID<5> IN 43 66
PMBUS_DATA	2	SDA	IPD VID4	24	VREG_CPU_VID<4> IN 43 66
VREG_CPU_PHASE2_R	17	SW2	IPD VID3	25	VREG_CPU_VID<3> IN 43 66
VREG_CPU_PHASE1_R	18	SW1	IPD VID2	26	VREG_CPU_VID<2> IN 43 66
VREG_CPU_CSCOMP	14	CSCOMP	IPD VID1	27	VREG_CPU_VID<1> IN 43 66
VREG_CPU_CSSUM	13	CSSUM	PWM2	19	VREG_CPU_PWM2 OUT 45
VREG_CPU_CSREF	12	CSREF	PWM1	20	VREG_CPU_PWM1 OUT 45
VREG_CPU_FB	11	FB	OD1_N	16	VREG_CPU_DRV_EN OUT 45
VREG_CPU_COMP	10	COMP	IMON	5	VREG_CPU_IMON
VREG_CPU_FBRTN	9	FBRTN	RT	7	VREG_CPU_RT
VREG_CPU_IREF	6	IREF			
VREG_CPU_ILIMITFS	15	ILIMITFS	MPAD	29	

R7C27 10 KOHM 1% 402 CH 1/16W
R7C28 909 KOHM 1% 402 CH 1/16W X812815-001
ROSC=909K
FOSC=250KHZ
R7C29 121 KOHM 1% 402 CH 1/16W
NEED TO SET DURING VALIDATION
PARTS ARE TRIMMED AT FACTORY SUCH THAT VBOOT=1.05V

I2C ADDRESS
1100 000 R/W HEX
WRITE 1100 000 0 0XC0
READ 1100 000 1 0XC1

C7C21 0.1 UF 10% 6.3 V X5R 402
R7C30 5.76 KOHM 1% 402 CH 1/16W
VREG_CPU_FBRTN
NOTE: VALID UP TO 58A
C7C19 1000 PF 10% 50 V X7R 402

[PAGE_TITLE=VREGS, CPU CONTROLLER]

DRAWING
Wed Mar 14 01:47:58 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	44/74	B	1.0

VREG, CPU OUTPUT PHASE 1 & 2

44 43 IN V_VREG_CPU

R6N1 1 2 2.2 OHM 1% 805 CH — VREG_CPU2_VCC

C6B4 1 UF 10% 16 V X5R 603

D6B1 SOT23 DIO

VREG_CPU_BST2

C6N1 1 2 0.01 UF 10% 50 V EMPTY 805

R6N2 1 2 2.2 OHM 1% 805 CH — VREG_CPU_BST2_R

C6N2 0.1 UF 10% 25 V X7R 603

U6B1 IC — MOS DRIVER

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

X850497-001

44 IN VREG_CPU_PWM2

44 IN VREG_CPU_DRV_EN

VREG_CPU_DRVH2

VREG_CPU_DRVL2

Q6B2 X857866-001 DPAK_G1D2S3 FET

Q6C2 X857867-001 DPAK_G1D2S3 FET

Q6C1 X857867-001 DPAK_G1D2S3 FET

C7B5 4.7 UF 10% 16 V X5R 1206

C7N1 4.7 UF 10% 16 V EMPTY 1206

R6C1 1 OHM 1% CH 805 — VREG_CPU_SW2_R

C7C8 2200 PF 10% 50 V X7R 805

VREG_CPU_PHASE2 OUT 44

V_CPUCORE
NOM.VOLTAGE: 0.9-1.2V

V_CPUCORE

L6C1 SM EMPTY DUAL INDUCTOR (L1 L4 L3 L2) — 1 DB7C4

X820048-001
420NH

DCR +/-8%

V_CPUCORE

L6C2 IND DUAL INDUCTOR (L2 L3 L4 L1)

X850592-001
420NH
40 A
0.00066DCR
+/-4%

NOTE: THRUHOLE PART IS 2% IMPROVEMENT ON DCR

R5N7 1 2 2.2 OHM 1% 805 CH — VREG_CPU1_VCC

C5B10 1 UF 10% 16 V X5R 603

D5B1 SOT23 DIO

VREG_CPU_BST1

C5N5 1 2 0.01 UF 10% 50 V EMPTY 805

R5N8 1 2 2.2 OHM 1% 805 CH — VREG_CPU_BST1_R

C5N6 0.1 UF 10% 25 V X7R 603

U5B5 IC — MOS DRIVER

4	VCC	BST	1
2	IN	DRVH	8
3	OD_N*	SW	7
6	PGND	DRVL	5

X850497-001

44 IN VREG_CPU_PWM1

VREG_CPU_DRVH1

VREG_CPU_DRVL1

Q6B1 X857866-001 DPAK_G1D2S3 FET

Q5C3 X857867-001 DPAK_G1D2S3 FET

Q5C1 X857867-001 DPAK_G1D2S3 FET

C6B2 4.7 UF 10% 16 V X5R 1206

C6N3 4.7 UF 10% 16 V EMPTY 1206

R5C1 1 OHM 1% CH 805 — VREG_CPU_SW1_R

C5C1 2200 PF 10% 50 V X7R 805

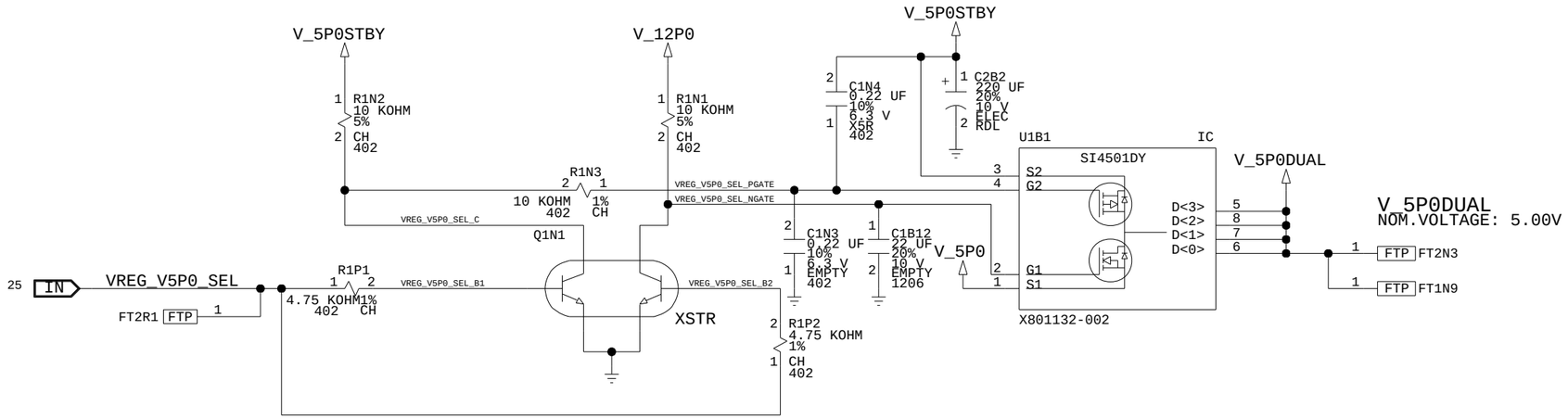
VREG_CPU_PHASE1 OUT 44

[PAGE_TITLE=VREGS, CPU OUTPUT PHASE 1,2]

DRAWING
Wed Mar 14 01:47:59 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	45/74	B	1.0

VREGS, V5P0 DUAL



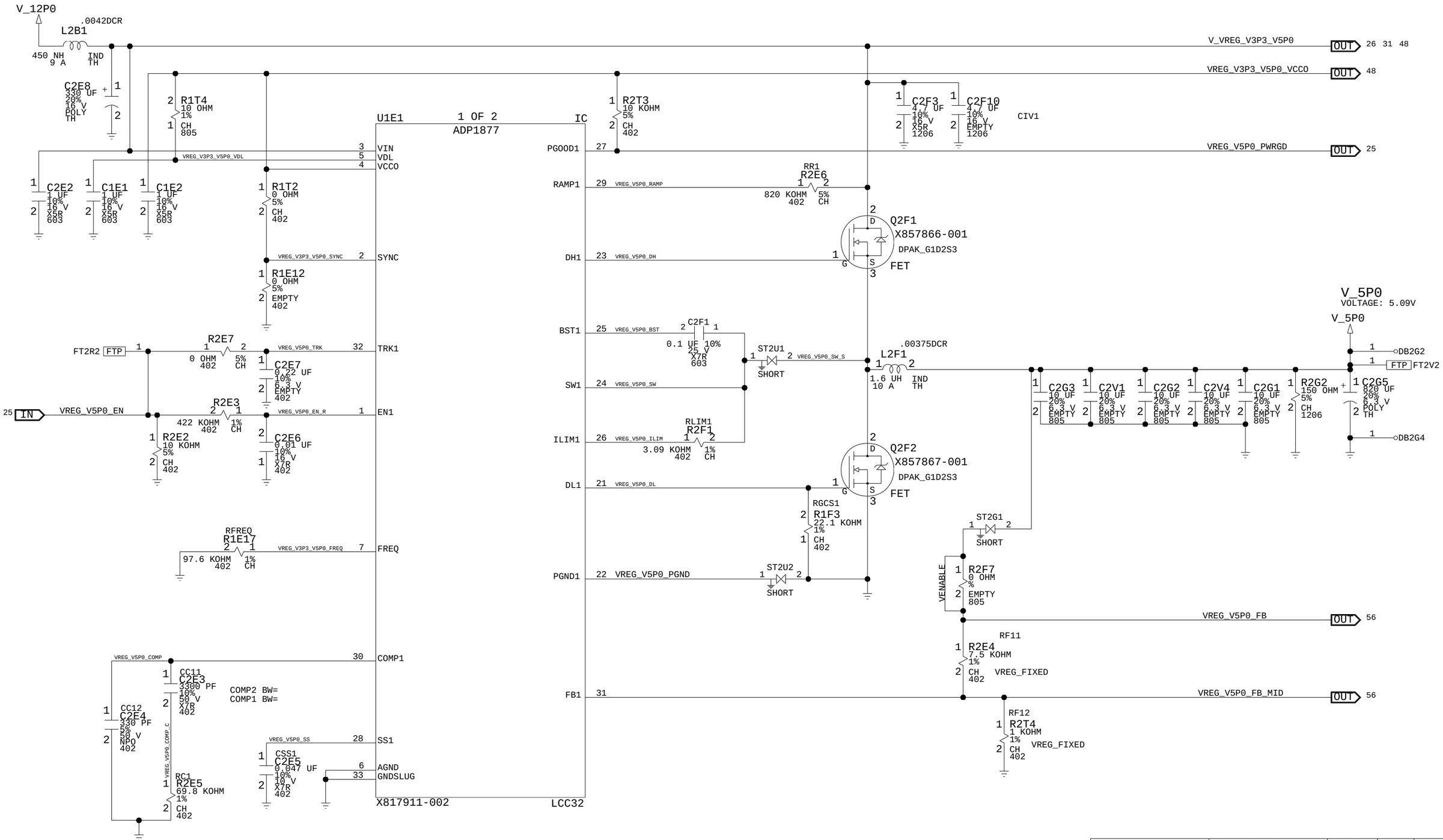
VREG_5P0_SEL	VREG_5P0_SEL NGATE/PGATE	V_5P0DUAL
HIGH	LOW	V_5P0STBY
LOW	HIGH	V_5P0

[PAGE_TITLE=VREGS, V5P0 DUAL]

DRAWING
Wed Mar 14 01:47:59 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 46/74	FAB B	REV 1.0

VREGS, V5P0

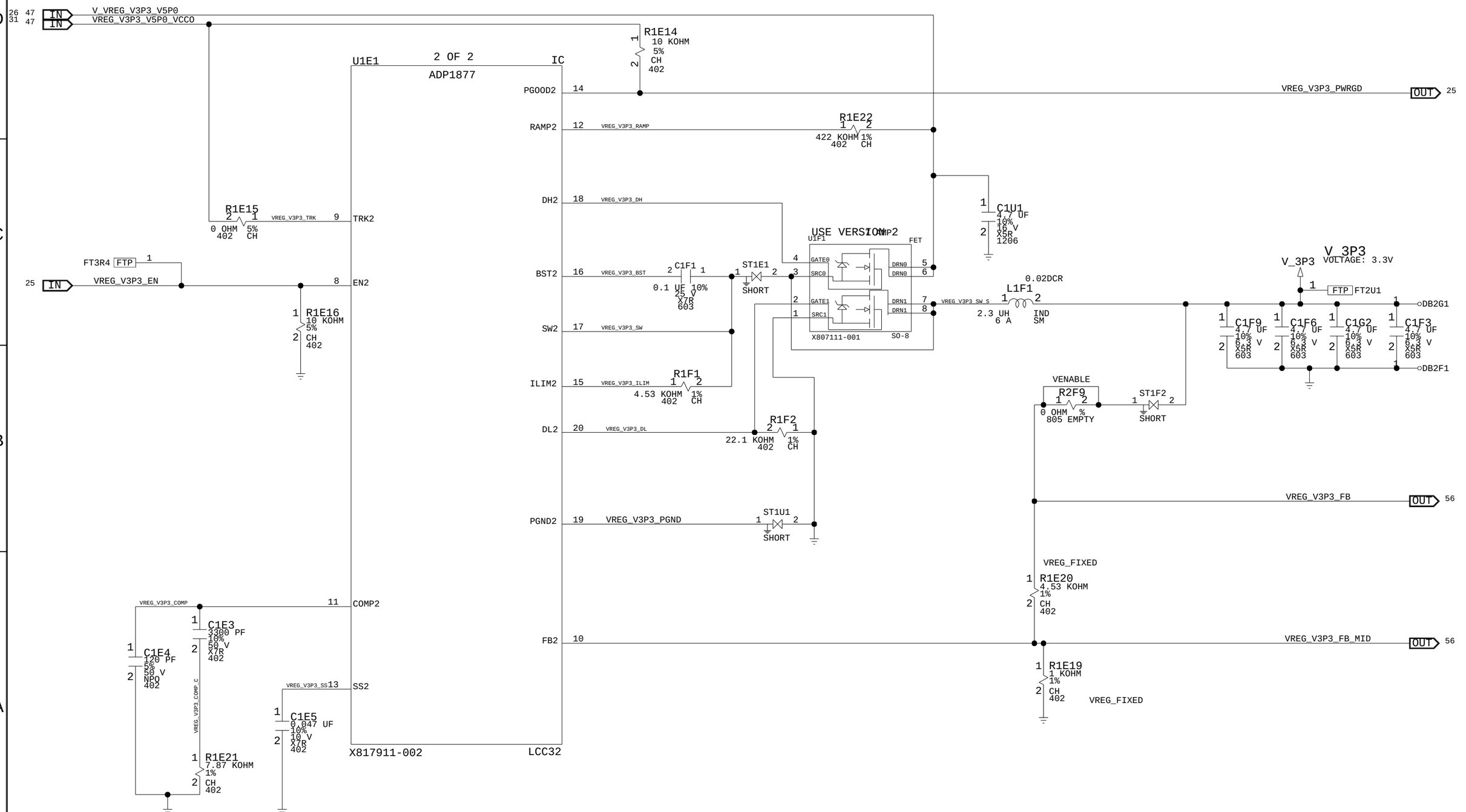


[PAGE_TITLE=VREGS, V5P0]

DRAWING
Wed Mar 14 01:47:59 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	47/74	B	1.0

VREGS, V3P3



[PAGE_TITLE=VREGS, V3P3]

DRAWING
Wed Mar 14 01:48:00 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	48/74	B	1.0

VREGS, VEDRAM

V_12P0
L7B1 .0042DCR
450 NH 9 A IND TH
C3F8 330 UF 20% 16 V POLY TH
C7B8 470 UF 20% 16 V POLY TH
R3G2 10 OHM 1% CH 805
U3G1 1 OF 2 ADP1877 IC
R3G16 10 KOHM 5% CH 402
C3F1 4.7 UF 10% 16 V X5R 1206
C3F7 4.7 UF 10% 16 V EMPTY 1206 CIV1
V_VREG_VMEM_VEDRAM OUT 50
VREG_VMEM_VEDRAM_VCCO OUT 50
VREG_VEDRAM_PWRGD OUT 25
VIN VDL VCCO
VREG_VMEM_VEDRAM_VDL
C3G1 1 UF 10% 16 V X5R 603
C3G3 1 UF 10% 16 V X5R 603
C3V1 1 UF 10% 16 V X5R 603
SYNC HIGH=FORCED PWM MODE
SYNC LOW =PULSE SKIP MODE
R3F12 0 OHM 5% CH 402
R3F14 0 OHM 5% CH 402
R3F13 0 OHM 5% EMPTY 402
VREG_VMEM_VEDRAM_SYNC SYNC
VREG_VEDRAM_TRK TRK1
PGOOD1 RAMP1 DH1 BST1 SW1 ILIM1 DL1 PGND1
VREG_VEDRAM_RAMP
RR1 R3F10 475 KOHM 1% 402 CH
Q3F1 X857866-001 DPAK_G1D2S3 FET
VREG_VEDRAM_DH
V_CPUEDRAM
V_CPUEDRAM VOLTAGE: 1.075V
FTP FT4T2
DB4E3
L4F1 .0034DCR 1.7 UH 13.8 A IND TH
C3F5 0.1 UF 10% 25 V X7R 603
ST3F1 SHORT
VREG_VEDRAM_BST VREG_VEDRAM_SW_S VREG_VEDRAM_SW
C4E3 820 UF 20% 2.5 V POLY RDL
C4E6 820 UF 20% 2.5 V EMPTY RDL
C4F7 820 UF 20% 2.5 V EMPTY RDL
C5T52 4.7 UF 10% 16 V EMPTY 1206
C5E11 4.7 UF 10% 16 V EMPTY 1206
C4T7 4.7 UF 10% 16 V EMPTY 1206
C5E10 4.7 UF 10% 16 V EMPTY 1206
RLIM1 R3F7 3.09 KOHM 1% 402 CH
VREG_VEDRAM_ILIM
Q4F1 X857867-001 DPAK_G1D2S3 FET
VREG_VEDRAM_DL
RGCS1 R3V1 22.1 KOHM 1% EMPTY 402
ST4U1 SHORT
VREG_VEDRAM_PGND
ST5E1 SHORT
DB4E4 DB4E5
VENABLE
R3F11 0 OHM EMPTY 805
VREG_VEDRAM_FB OUT 55
RF11 R3F8 7.87 KOHM 1% CH 402 VREG_FIXED
VREG_VEDRAM_FB_MID OUT 55
RF12 R3F9 10 KOHM 1% CH 402 VREG_FIXED
FT2T9 FTP
25 IN VREG_VEDRAM_EN
R3F15 10 KOHM 5% CH 402
EN1
RFREQ R3G4 97.6 KOHM 1% 402 CH
VREG_VEDRAM_FREQ FREQ
VREG_VEDRAM_COMP COMP1
CC11 C3F2 1000 PF 10% 50 V X7R 402
CC12 C3F3 10 PF 5% 50 V NPO 402
RC1 R3F6 169 KOHM 1% CH 402
RC1=120K
VREG_VEDRAM_SS SS1
CSS1 C3F4 0.047 UF 10% 10 V X7R 402
AGND GNDSLUG
X817911-002 LCC32

[PAGE_TITLE=[VREGS, VEDRAM]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	49/74	B	1.0

VREGS, VMEM

49 IN V_VREG_VMEM_VEDRAM

49 IN VREG_VMEM_VEDRAM_VCCO

U3G1 2 OF 2 IC
ADP1877

R3G15 10 KOHM 5% CH 402

CIV2 C7F3 4.7 UF 10% 16 V X5R 1206

C7U1 4.7 UF 10% 16 V EMPTY 1206

PGOOD2 14 VREG_VMEM_PWRGD OUT 25

RAMP2 12 VREG_VMEM_RAMP

RR2 R3G13 422 KOHM 1% 402 CH

Q7G1 X857866-001 DPAK_G1D2S3 FET

DH2 18 VREG_VMEM_DH

R3G5 0 OHM 5% 402 CH

VREG_VMEM_TRK 9 TRK2

V_MEM VOLTAGE: 1.8V

DB7F1

FTP FT7U1

V_MEM

.0034DCR L7F1 IND 1.7 UH TH 13.8 A

FT2T1 FTP 1

25 IN VREG_VMEM_EN 8 EN2

R3G14 10 KOHM 5% CH 402

BST2 16 VREG_VMEM_BST

C3G9 0.1 UF 10% 25 V X7R 603

ST6V2 SHORT

VREG_VMEM_SW_S

C7F2 820 UF 20% 2.5 V POLY RDL

C7F1 4.7 UF 10% 6.3 V EMPTY 603

DB7F2

SW2 17 VREG_VMEM_SW

V_MEM

C7R1 330 UF 20% 2.5 V EMPTY SM

RLIM2 R3G10 3.09 KOHM 1% 402 CH

ILIM2 15 VREG_VMEM_ILIM

Q7G2 X857867-001 DPAK_G1D2S3 FET

DL2 20 VREG_VMEM_DL

V_MEM

C4U4 330 UF 20% 2.5 V EMPTY SM

RGCS2 R4G3 22.1 KOHM 1% EMPTY 402

ST7F1 SHORT

PGND2 19 VREG_VMEM_PGND

ST6V1 SHORT

VENABLE R3G17 0 OHM EMPTY 805

VREG_VMEM_FB OUT 55

RF21 VREG_FIXED R3G11 20 KOHM 1% CH 402

FB2 10

VREG_VMEM_FB_MID OUT 55

RF22 VREG_FIXED R3G12 10 KOHM 1% CH 402

VREG_VMEM_COMP 11 COMP2

CC21 C3G6 1000 PF 10% 50 V X7R 402

CC22 C3G7 47 PF 5% 50 V NPO 402

VREG_VMEM_COMP_C

RC2 R3V4 169 KOHM 1% CH 402

VREG_VMEM_SS 13 SS2

CSS1 C3G8 0.047 UF 10% 10 V X7R 402

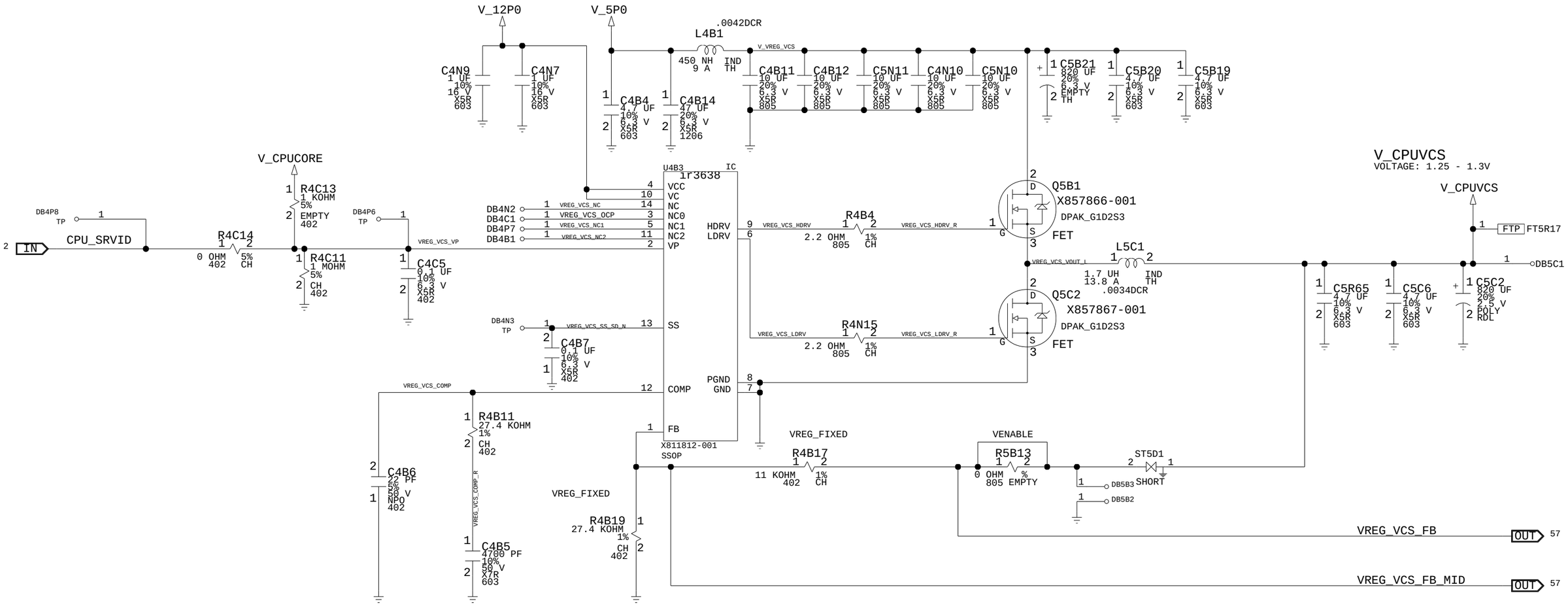
X817911-002 LCC32

[PAGE_TITLE=[VREGS, VMEM]

DRAWING
Wed Mar 14 01:48:01 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	50/74	B	1.0

VREGS, VCS



GAIN=0.4 WITH R4B17 = 11K, R4B19 = 27.4K
OUTPUT = CPU_SRVID(1+GAIN)

[PAGE_TITLE=VREGS, VCS]

DRAWING
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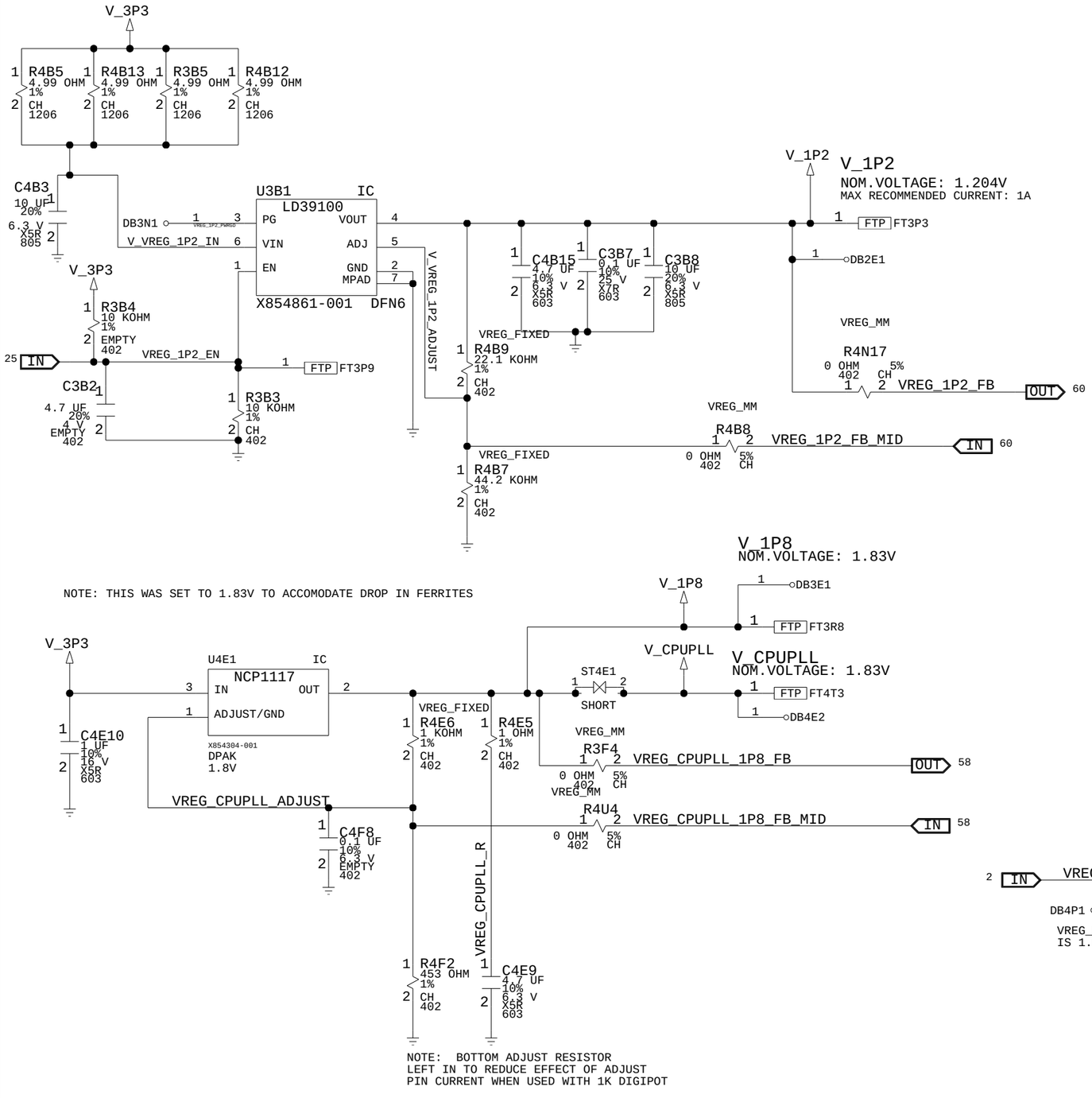
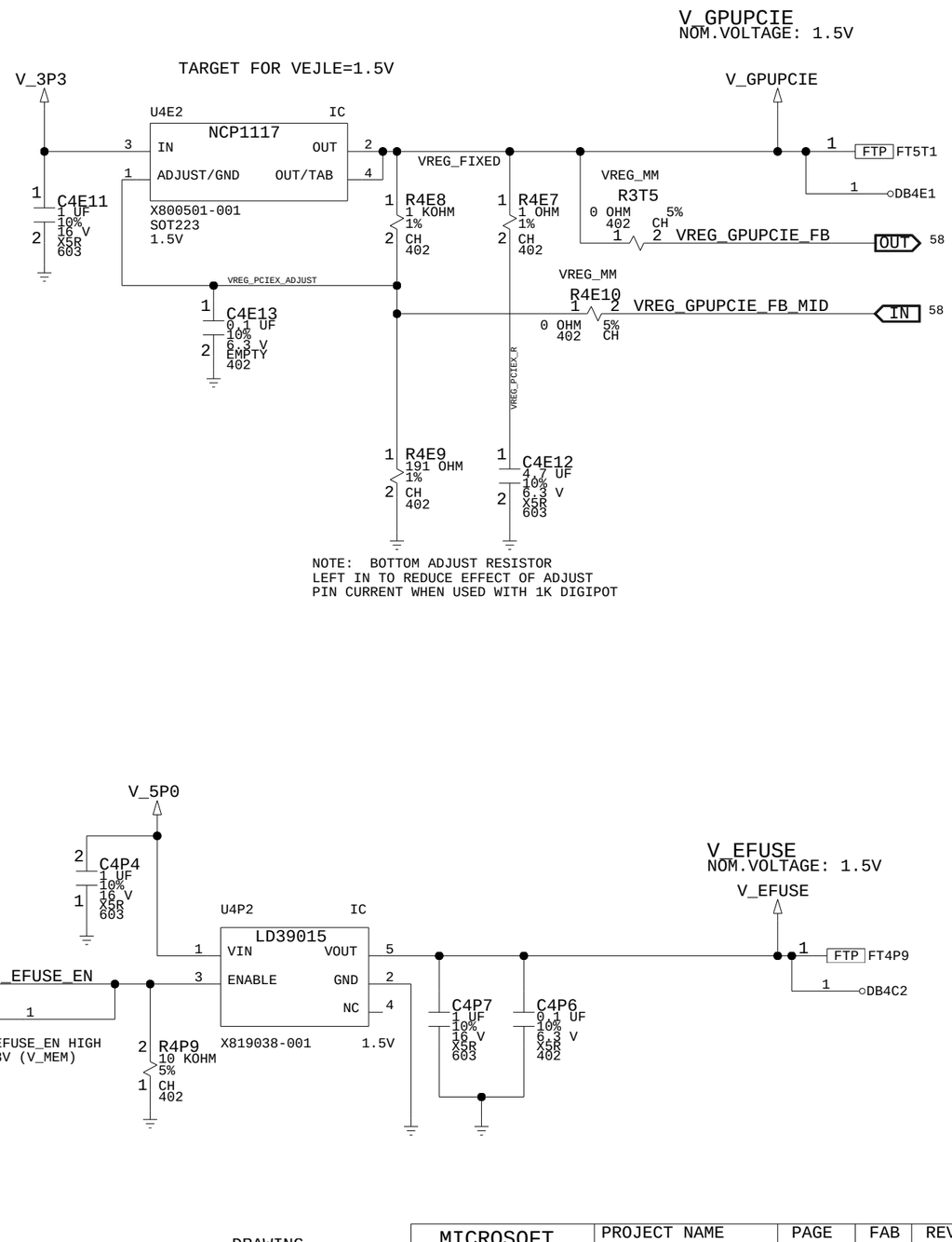
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	51/74	B	1.0

VREGS, 1P2+1P8+GPUPCIE+CPUPLL+EFUSE





[PAGE_TITLE=VREGS, 1P8+GPUPCIE+SBPCIE+CPUPLL+EFUSE]

DRAWING
Wed Mar 14 01:48:02 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	52/74	B	1.0

VREGS,STANDBY SWITCHERS

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R5B5	X855279-001	CH	RES,42.2K,0402	VREG_MM
C5B1	X800440-001	NPO	CAP,75PF,0402	VREG_MM
R5A15	X800467-001	CH	RES,30.1K,0402	VREG_MM

PACK_IGNORE=TRUE

FIXED VS. M&M COMPONENTS

REF DES	FIXED	M&M
C5B1	33PF	75PF
R5A15	178KOHM	30.1KOHM
R5A5	178KOHM	22.1KOHM
R5A6	806KOHM	100KOHM
R5B5	249KOHM	42.2KOHM

V_1P2STBY
NOM.VOLTAGE: 1.2V
MAX RECOMMENDED CURRENT: 300MA

V_5P0STBY
0.08DCR
L5B1
2.2 UH 1.6 A IND 1210
0.05 OHM
C5M9 10 UF 20% 6.3 V X5R 805
C5A4 10 UF 20% 6.3 V X5R 805
C5A5 10 UF 20% 6.3 V X5R 805
FT5M3 FTP
V_VREG_STBY_VIN
U5A2 IC TPS62220
X855078-001 SOT23-5
IN SW FB EN GND
VREG_1P2STBY_SW
L5B2 10 UH 900 MA IND SM
VREG_FIXED
DB5B1
DB3C2
C5B2 10 UF 20% 6.3 V X5R 805
C5B7 4.7 UF 10% 6.3 V EMPTY 603
C5B3 0.1 UF 10% 25 V X7R 603
DB5N1
V_3P3STBY
R5A4 10 KOHM 1% CH 402
R5A7 10 KOHM 1% EMPTY 402
VREG_1P2STBY_EN
C5M8 10 UF 20% 6.3 V EMPTY 805
DB5M2
VREG_1P2STBY_FB_CHIP
R5A15 178 KOHM 1% CH 402
C5A9 100 PF 5% 50 V EMPTY 402
R5B5 249 KOHM 1% 402 CH VREG_FIXED
C5B1 33 PF 5% 50 V NPO 402
VENABLE
R5B4 0 OHM 5% 402 EMPTY
ST3C6 SHORT
VREG_MM
VREG_1P2STBY_FB_R
R5B2 0 OHM 5% 402 CH
VREG_1P2STBY_FB
OUT 59
R5A13 0 OHM 5% 402 CH
VREG_1P2STBY_FB_MID
IN 59

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
R5A6	X802226-001	CH	RES,100K,0402	VREG_MM
C5A1	X801069-001	NPO	CAP,22PF,0402	VREG_MM
R5A5	X801153-001	CH	RES,22.1K,0402	VREG_MM

PACK_IGNORE=TRUE

V_3P3STBY
NOM.VOLTAGE: 3.315V
MAX RECOMMENDED CURRENT: 1A

V_1P2STBY
R5M6 10 KOHM 1% EMPTY 402
R5M9 10 KOHM 1% CH 402
VREG_3P3STBY_EN
C5M5 4.7 UF 10% 6.3 V EMPTY 603
DB5M3 TP
U5A1 IC TPS62590
X854683-001 DFN6
IN EN MODE SW FB GND MPAD
VREG_3P3STBY_SW
L5A1 0.08DCR 2.2 UH 1.6 A IND 1210
VREG_FIXED
DB5M1
V_3P3STBY
DB5A2
VREG_3P3STBY_FB_CHIP
R5A6 806 KOHM 1% 402 CH
C5A2 10 UF 20% 6.3 V X5R 805
C5A3 0.1 UF 10% 25 V X7R 603
DB5A1
R5A5 178 KOHM 1% CH 402
C5A1 22 PF 5% 50 V NPO 402
VENABLE
R5A3 0 OHM 5% 402 EMPTY
ST2D1 SHORT
VREG_MM
VREG_3P3STBY_FB_R
R5A8 0 OHM 5% 402 CH
VREG_3P3STBY_FB
OUT 59
R5A12 0 OHM 5% 402 CH
VREG_3P3STBY_FB_MID
IN 59

R5A5 SHOULD BE 182KOHM 0402, WAITING ON COMPONENT TB ADDED IN TC

[PAGE_TITLE=VREGS, STANDBY SWITCHERS]

DRAWING
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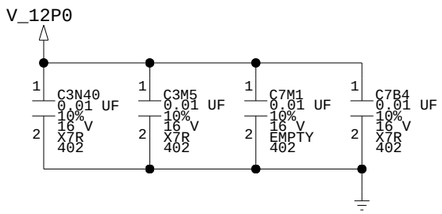
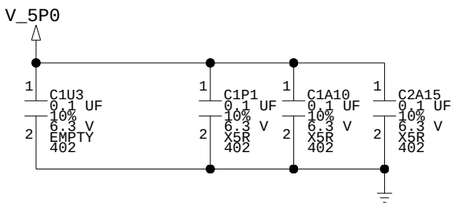
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	53/74	B	1.0

BOARD LEVEL DECOUPLING

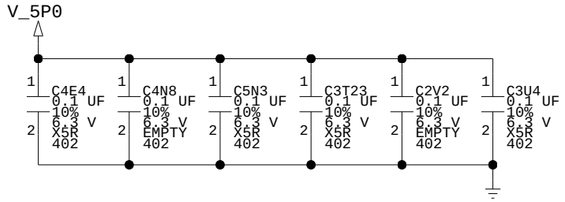
V_12P0



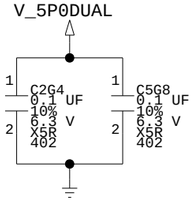
V_5P0



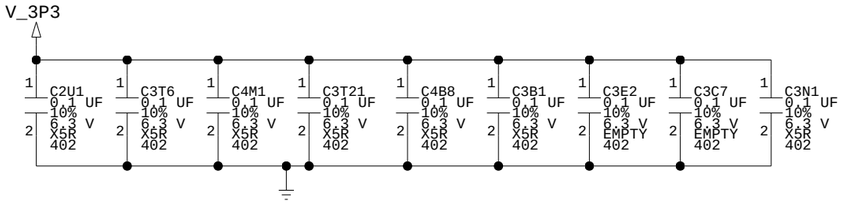
V_5P0



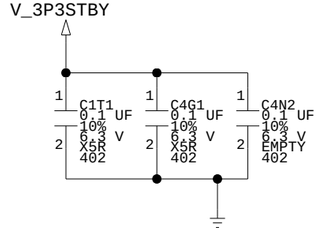
V_5P0DUAL



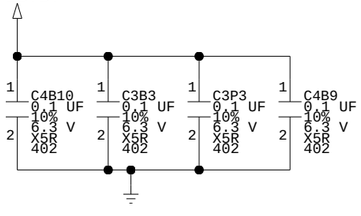
V_3P3



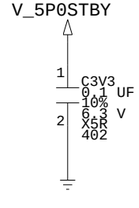
V_3P3STBY



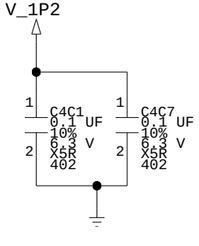
V_1P2STBY



V_5P0STBY



V_1P2



[PAGE_TITLE=BOARD, DECOUPLE]

DRAWING
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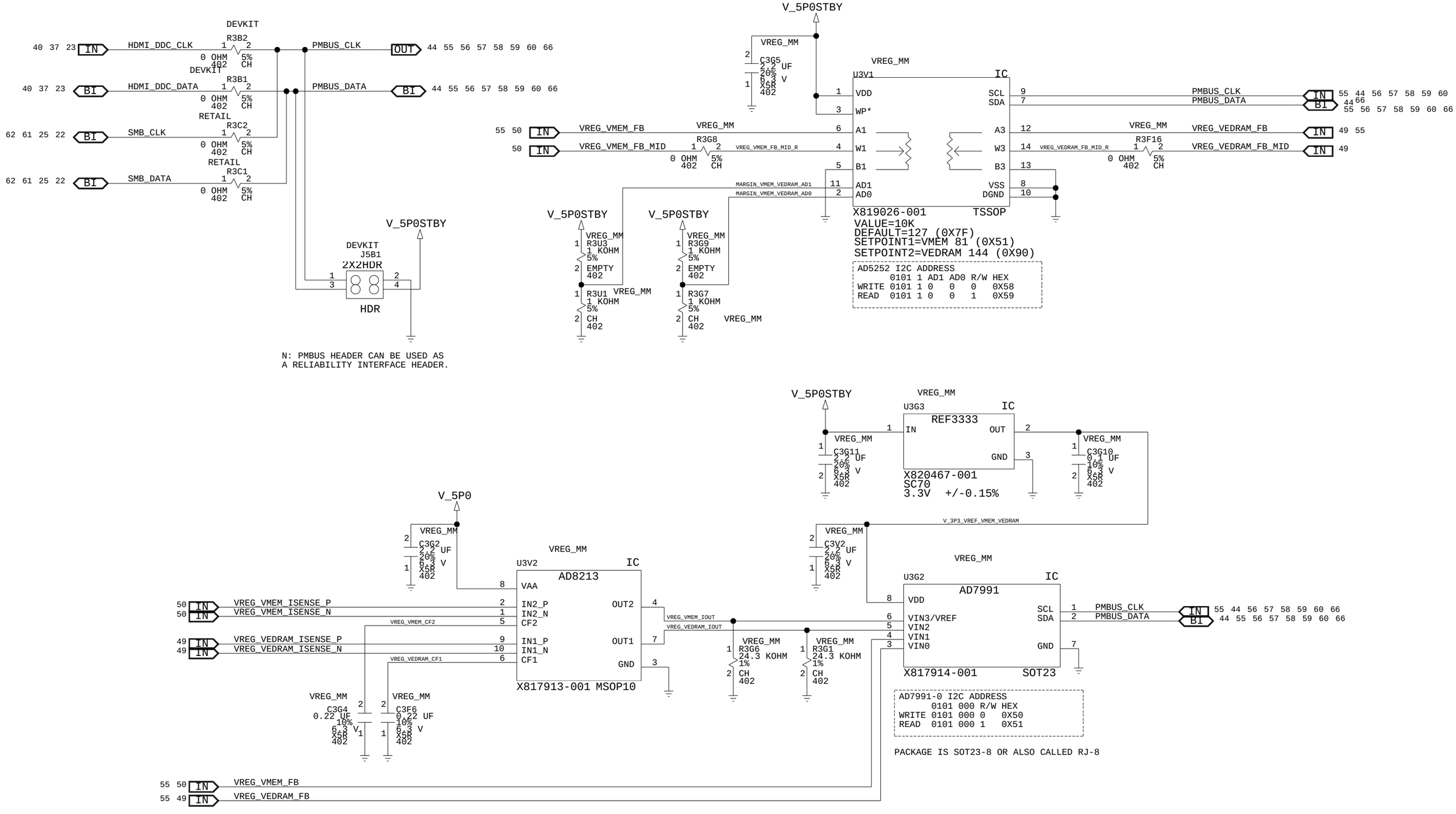
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	54/74	B	1.0

MARGIN, VMEM + VEDRAM



[PAGE_TITLE=MARGIN, VMEM + VEDRAM]

DRAWING
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	55/74	B	1.0

MARGIN, V3P3 + V5P0

47 IN VREG_V5P0_FB
VREG_MM R2U1 35.7 KOHM 1% 2 CH 402
VREG_MM Q2F3 ADR5043 N(3) X819033-001 3.0V 0.1% V N IC
V_5P0STBY
VREG_MM C2F4 2.2 UF 20% 6.3 V X5R 402
VREG_MM
U1U1 IC
1 VDD
3 WP*
6 A1
4 W1
5 B1
11 AD1
2 AD0
SCL 9 PMBUS_CLK
SDA 7 PMBUS_DATA
IN 59 60 66 55 44 56 57 58
B1 44 55 56 57 58 59 60 66
A3 12 VREG_V3P3_FB_A3
W3 14 VREG_V3P3_FB_MID_R
VSS 8
DGND 10
X819026-001 TSSOP
VALUE=10K
DEFAULT=128 (0X7F)
SETPOINT1=V5P0 69 (0X45)
SETPOINT2=V3P3 123 (0X7B)

VREG_MM Q1F1 N(3) X819034-001 2.048V 0.1% V N IC ADR5040A
VREG_MM R1U5 22.1 KOHM 1% 2 CH 402
VREG_V3P3_FB IN 48
VREG_MM R1T19 0 OHM 5% 402 CH
VREG_V3P3_FB_MID IN 48

47 IN VREG_V5P0_FB_MID
VREG_MM R2T5 0 OHM 5% 402 CH
VREG_V5P0_FB_A1
VREG_V5P0_FB_MID_R
MARGIN_V3P3_V5P0_AD1
MARGIN_V3P3_V5P0_AD0

V_5P0STBY
VREG_MM R1U4 1 KOHM 5% 2 EMPTY 402
VREG_MM R1U3 1 KOHM 5% 2 CH 402
VREG_MM
V_5P0STBY
VREG_MM R2F3 1 KOHM 5% 2 CH 402
VREG_MM R2F2 1 KOHM 5% 2 EMPTY 402

AD5252 I2C ADDRESS
0101 1 AD1 AD0 R/W HEX
WRITE 0101 1 0 1 0 0X5A
READ 0101 1 0 1 1 0X5B

V_5P0DUAL
VREG_MM C1F10 2.2 UF 20% 6.3 V X5R 402
VREG_MM U1F3 IC REF3333 IN 1 OUT 2 GND 3
X820467-001 SC70 3.3V +/-0.15%
VREG_MM C1F11 0.1 UF 10% 6.3 V X5R 402
V_3P3_VREF_V5P0_V3P3

V_5P0
VREG_MM C1U2 2.2 UF 20% 6.3 V X5R 402
VREG_MM U2U1 IC AD8213
8 VAA
47 IN VREG_V5P0_ISENSE_P
47 IN VREG_V5P0_ISENSE_N
2 IN2_P
1 IN2_N
5 CF2
48 IN VREG_V3P3_ISENSE_P
48 IN VREG_V3P3_ISENSE_N
9 IN1_P
10 IN1_N
6 CF1
OUT2 4
OUT1 7
GND 3
VREG_V5P0_IOUT
VREG_V3P3_IOUT
VREG_V5P0_CF2
VREG_V3P3_CF1
VREG_MM C2F6 0.22 UF 10% 6.3 V X5R 402
VREG_MM C1F2 0.22 UF 10% 6.3 V X5R 402
X817913-001 MSOP10

VREG_MM R2F5 24.3 KOHM 1% 2 CH 402
VREG_MM R2F8 24.3 KOHM 1% 2 CH 402

VREG_MM U1F2 IC AD7991
8 VDD
6 VIN3/VREF
5 VIN2
4 VIN1
3 VIN0
SCL 1 PMBUS_CLK
SDA 2 PMBUS_DATA
GND 7
X818998-001 SOT23
IN 55 44 56 57 58 59 60 66
B1 44 55 56 57 58 59 60 66

AD7991-1 I2C ADDRESS
0101 001 R/W HEX
WRITE 0101 001 0 0X52
READ 0101 001 1 0X53

PACKAGE IS SOT23-8 OR ALSO CALLED RJ-8

V_5P0
VREG_MM R2F4 150 OHM 1% 402 CH
VREG_V5P0_FB_R
V_3P3
VREG_MM R1F4 150 OHM 1% 402 CH
VREG_V3P3_FB_R

VREG_MM R1F6 221 OHM 1% 2 CH 402
VREG_MM R1F5 221 OHM 1% 2 CH 402

[PAGE_TITLE=MARGIN, V3P3 + VP50]

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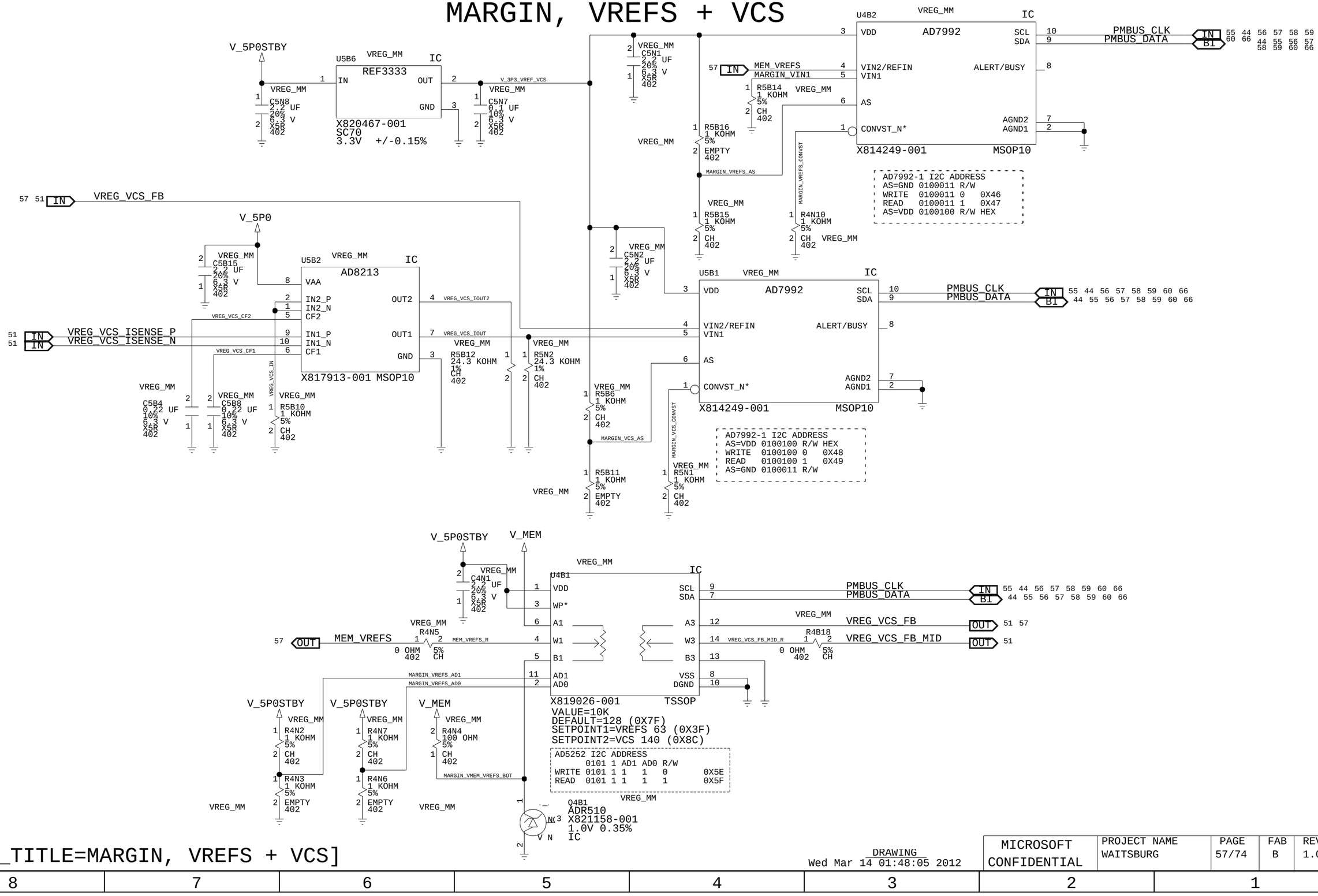
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	56/74	B	1.0

MARGIN, VREFS + VCS



[PAGE_TITLE=MARGIN, VREFS + VCS]

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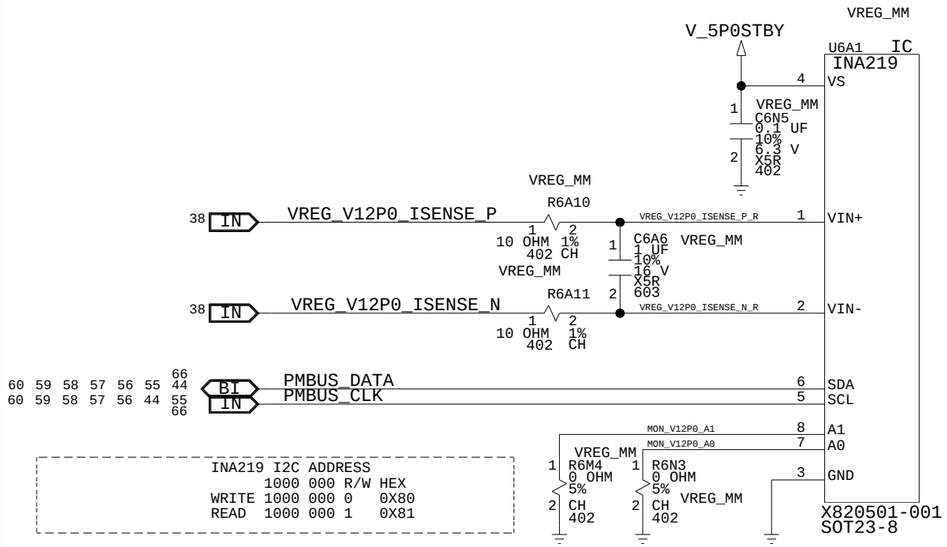
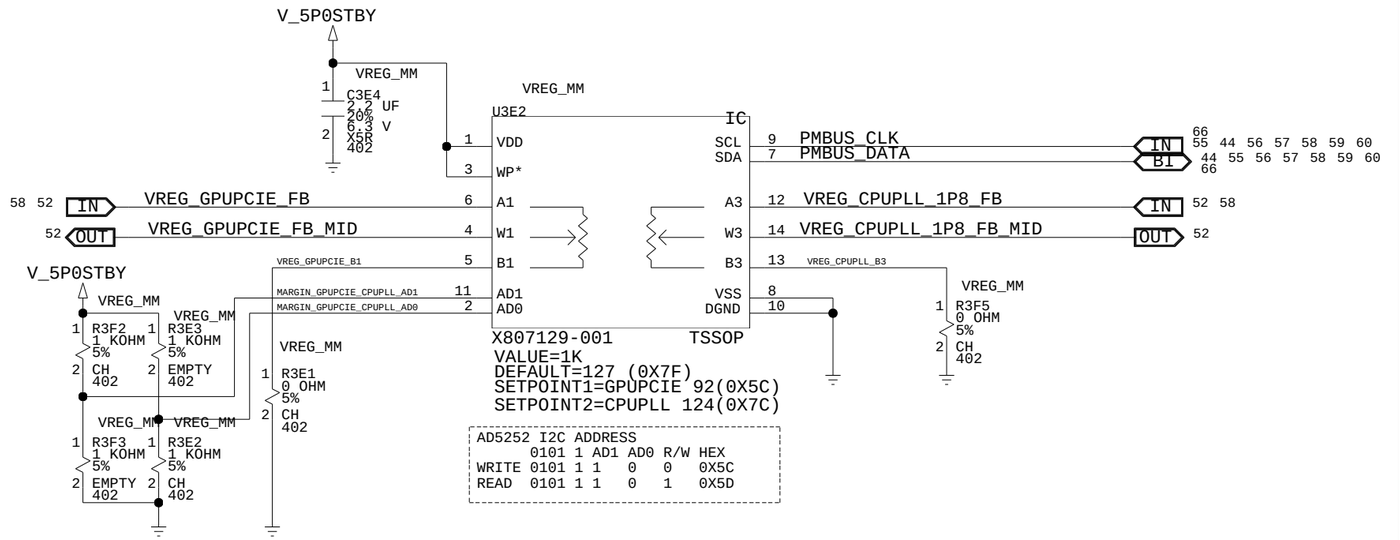
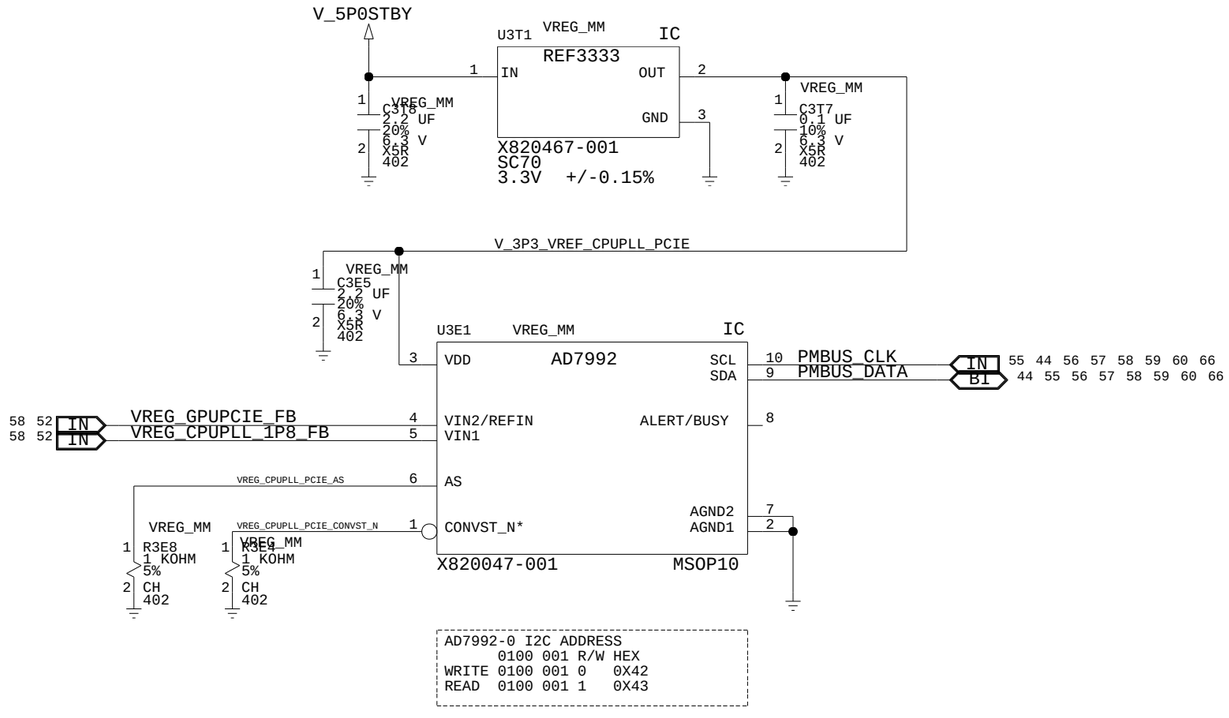
Wed Mar 14 01:48:05 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	57/74	B	1.0

MARGIN, VGPUPCIE,1P8, VCPUPLL, V12P0, TEMP







[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	58/74	B	1.0

MARGIN, STANDBY

INA219 I2C ADDRESS
1001 100 R/W HEX
WRITE 1001 100 0 0X98
READ 1001 100 1 0X99

V_5P0STBY
VREG_MM
U5N3 IC INA219
VS
C6N6 0.1 UF 10% 6.3 V X5R 402
38 IN V5P0STBY_ISENSE_P
R6N4 10 OHM 1% 402 CH
V5P0STBY_ISENSE_P_R
VIN+
C6N4 1 UF 10% 16 V X5R 603
38 IN V5P0STBY_ISENSE_N
R6N5 10 OHM 1% 402 CH
V5P0STBY_ISENSE_N_R
VIN-
60 59 58 57 56 55 44 66 BI PMBUS_DATA
60 59 58 57 56 44 55 66 IN PMBUS_CLK
SDA
SCL
R5N5 3.32 KOHM 1% 402 CH
MON_V5P0STBY_A1
A1
MON_V5P0STBY_A0
A0
R5N3 0 OHM 5% 402 CH
GND
X820501-001
SOT23-8

V_5P0STBY
VREG_MM
R5A14 1 KOHM 5% 402 CH
53 IN VREG_1P2STBY_FB
R5B1 20 KOHM 1% 402 CH
VREG_1P2STBY_FB_D
53 OUT VREG_1P2STBY_FB_MID
U5A3 IC MCP4661
P1B
P1W
P1A
60 59 58 57 56 44 55 66 IN PMBUS_CLK
59 58 57 56 55 44 66 60 BI PMBUS_DATA
SCL
SDA
MARGIN_STBY_A2
MARGIN_STBY_A1
MARGIN_STBY_A0
A2
A1
HVC/A0
R5M14 1 KOHM 5% 402 CH
R5B3 1 KOHM 5% 402 CH
VREG_MM
X854038-001
VDD
WP_N
P0B
P0W
P0A
NC
VSS2
VSS
MPAD
C5N4 0.1 UF 10% 6.3 V X5R 402
R5M15 178 KOHM 1% 402 CH
VREG_3P3STBY_FB
53 IN
VREG_3P3STBY_FB_D
VREG_3P3STBY_FB_MID
53 OUT

MCP4661 I2C ADDRESS
0101 AD2 AD1 AD0 R/W HEX
WRITE 0101 0 1 0 0 0X54
READ 0101 0 1 0 1 0X55

BUGBUG: NEED TO DECIDE R VALUE
BUGBUG: FOR NOMINAL VOLTAGE OF 1.2V

INA219 I2C ADDRESS
1001 000 R/W HEX
WRITE 1001 001 0 0X92
READ 1001 001 1 0X93

V_5P0STBY
VREG_MM
U5M1 IC INA219
VS
C5M6 0.1 UF 10% 6.3 V X5R 402
53 IN V3P3STBY_ISENSE_P
R5M11 10 OHM 1% 402 CH
V3P3STBY_ISENSE_P_R
VIN+
C5M7 1 UF 10% 16 V X5R 603
53 IN V3P3STBY_ISENSE_N
R5M10 10 OHM 1% 402 CH
V3P3STBY_ISENSE_N_R
VIN-
66 60 59 58 57 56 55 44 BI PMBUS_DATA
66 60 59 58 57 56 44 55 IN PMBUS_CLK
SDA
SCL
R5M13 3.32 KOHM 1% 402 CH
MON_V3P3STBY_A1
A1
MON_V3P3STBY_A0
A0
GND
R5M12 0 OHM 5% 402 CH
X820501-001
SOT23-8

INA219 I2C ADDRESS
1000 011 R/W HEX
WRITE 1000 011 0 0X86
READ 1000 011 1 0X87

V_5P0STBY
VREG_MM
U5N2 IC INA219
VS
C5N9 0.1 UF 10% 6.3 V X5R 402
53 IN V1P2STBY_ISENSE_P
R5M16 10 OHM 1% 402 CH
V1P2STBY_ISENSE_P_R
VIN+
C5M10 1 UF 10% 16 V X5R 603
53 IN V1P2STBY_ISENSE_N
R5N4 10 OHM 1% 402 CH
V1P2STBY_ISENSE_N_R
VIN-
66 60 59 58 57 56 55 44 BI PMBUS_DATA
66 60 59 58 57 56 44 55 IN PMBUS_CLK
SDA
SCL
MON_V1P2STBY_A1
A1
MON_V1P2STBY_A0
A0
GND
R4N9 0 OHM 5% 402 CH
R4N11 3.32 KOHM 1% 402 CH
X820501-001
SOT23-8

[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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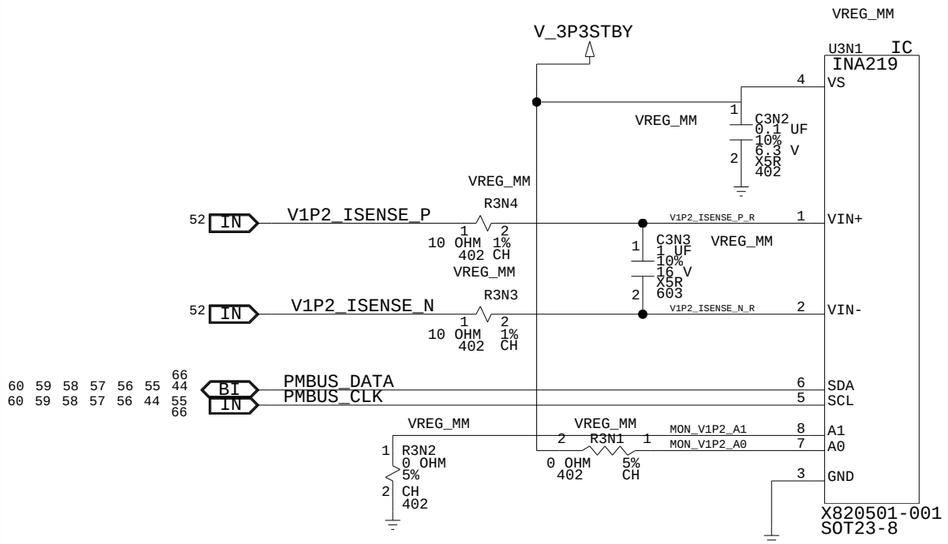
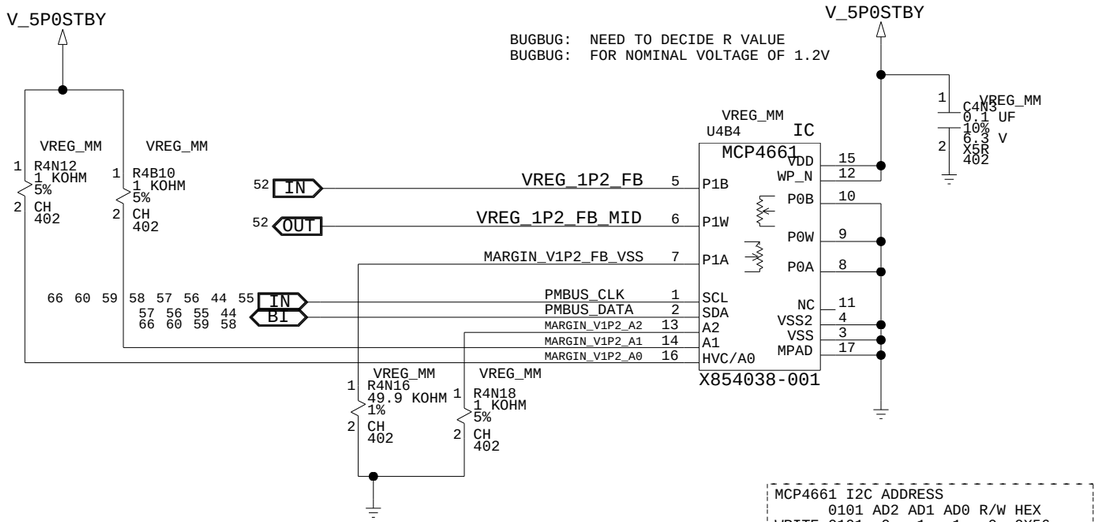
MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	59/74	B	1.0

MARGIN, V1P2



INA219 I2C ADDRESS					
	1000	100	R/W	HEX	
WRITE	1000	001	0	0X82	
READ	1000	001	1	0X83	



MCP4661 I2C ADDRESS						
	0101	AD2	AD1	AD0	R/W	HEX
WRITE	0101	0	1	1	0	0X56
READ	0101	0	1	1	1	0X57

[PAGE_TITLE=MARGIN, VGPUPCIE, VSBPCIE, VCPUPLL, V12P0, TEMP]

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MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 60/74	FAB B	REV 1.0

EXTERNAL TEMP SENSORS

ISOLATE CLOSE TO KSB

62 55 25 22 BI SMB_CLK 1 R3P7 2 SMB_CLK_EXTTEMP_R 1 R3R13 2 SMB_CLK_EXTTEMP BI 61
0 OHM 5% 402 CH JTM_EXT 0 OHM 5% 402 CH JTM_EXT

62 55 25 22 BI SMB_DATA 1 R3P6 2 SMB_DATA_EXTTEMP_R 1 R3R14 2 SMB_DATA_EXTTEMP BI 61
0 OHM 5% 402 CH JTM_EXT 0 OHM 5% 402 CH JTM_EXT

ISOLATE CLOSE TO EXT TEMP

4 OUT CPU_TEMP_P — 1 R4D7 2 CPU_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT
1 R4R28 2 CPU_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 23 66 (CPU_TEMP_P_KSB) OUT 61 (CPU_TEMP_P_EXT) C4D3 100 PF 5% 50 V EMPTY 402

4 OUT CPU_TEMP_N — 1 R4D8 2 CPU_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT
1 R4R29 2 CPU_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 66 23 (CPU_TEMP_N_KSB)

4 OUT GPU_TEMP_P — 1 R4D6 2 GPU_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT
1 R4R27 2 GPU_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 23 66 (GPU_TEMP_P_KSB) OUT 61 (GPU_TEMP_P_EXT) C4D2 100 PF 5% 50 V EMPTY 402

4 OUT GPU_TEMP_N — 1 R4D5 2 GPU_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT
1 R4R26 2 GPU_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 66 23 (GPU_TEMP_N_KSB)

ST4R1 2 1 SHORT
ST4D1 2 1 SHORT

38 23 OUT BRD_TEMP_P — 1 R3R18 2 BRD_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT
1 R3D30 2 BRD_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 23 (BRD_TEMP_P_KSB) OUT 61 (BRD_TEMP_P_EXT) 2 402 EMPTY 50 V 5% 1 100 PF C3R56

38 23 OUT BRD_TEMP_N — 1 R3R19 2 BRD_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT
1 R3D31 2 BRD_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 23 (BRD_TEMP_N_KSB)

ST4R2 2 1 SHORT

4 OUT EDRAM_TEMP_P — 1 R4D3 2 EDRAM_TEMP_P_KSB — 0 OHM 5% 402 CH JTM_INT
1 R4R24 2 EDRAM_TEMP_P_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 23 66 (EDRAM_TEMP_P_KSB) OUT 61 (EDRAM_TEMP_P_EXT) C4D1 100 PF 5% 50 V EMPTY 402

4 OUT EDRAM_TEMP_N — 1 R4D4 2 EDRAM_TEMP_N_KSB — 0 OHM 5% 402 CH JTM_INT
1 R4R25 2 EDRAM_TEMP_N_EXT — 0 OHM 5% 402 CH JTM_EXT
OUT 66 23 (EDRAM_TEMP_N_KSB)

61 IN CPU_TEMP_P_EXT — C4R4 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
61 IN GPU_TEMP_P_EXT — C4R5 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
61 IN BRD_TEMP_P_EXT — C4R1 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR
61 IN EDRAM_TEMP_P_EXT — C4R3 100 PF 5% 50 V EMPTY 402 PLACE CLOSE TO SENSOR

EXT_TEMP_N — 1 JTM_EXT R4R35 0 OHM 5% CH 402 2

R4R34 1 0 OHM 5% EMPTY 402 2

JTM_EXT R4R31 1 0 OHM 5% 2 CH 402
R4R30 1 0 OHM 5% 2 EMPTY 402
V_EXTTEMP
R4R33 1 0 OHM 5% 2 EMPTY 402
R4R32 1 0 OHM 5% 2 CH 402 JTM_EXT

JTM_EXT U4R1 IC TMP423 X858059-001 SOT23-8
1 DXP1 V+ 8 — JTM_EXT C4R2 0.1 UF 10% 6.3 V X5R 402 2 — V_EXTTEMP
2 DXP2 SCL 7 SMB_CLK_EXTTEMP BI 61
3 DXP3 SDA 6 SMB_DATA_EXTTEMP BI 61
4 DXN GND 5

TMP423B I2C ADDRESS
1001 100 R/W HEX
WRITE 1001 101 0 0X9A
READ 1001 101 1 0X9B

V_EXTTEMP
JTM_EXT U3R1 IC TMP441 X858003-001 SOT23-8
1 DXP V+ 8 — JTM_EXT C3D9 0.1 UF 10% 6.3 V X5R 402 2 — V_EXTTEMP
2 DXN SCL 7 SMB_CLK_EXTTEMP BI 61
3 A1 SDA 6 SMB_DATA_EXTTEMP BI 61
4 A0 GND 5
EXT_TMP_A1
EXT_TMP_A0

TMP441 I2C ADDRESS
10011 AD1 AD0 R/W HEX
WRITE 10011 1 0 0 0X9C
READ 10011 1 0 1 0X9D

V_EXTTEMP
25 IN EXT_TEMP_PWR_CTRL — 1 Q3R1 EMPTY 1.1 OHM SOT23 3 — 1 FTP FT3R18
1 R3R20 10 KOHM 1% EMPTY 402 2
1 JTM_EXT R4R36 0 OHM 5% CH 402 2 — V_3P3STBY

V_3P3STBY
JTM_EXT C3D10 0.1 UF 10% 6.3 V X5R 402 — JTM_EXT C3D11 0.1 UF 10% 6.3 V X5R 402
STITCHING CAPS FOR BRD_TEMP PLANE SPLIT

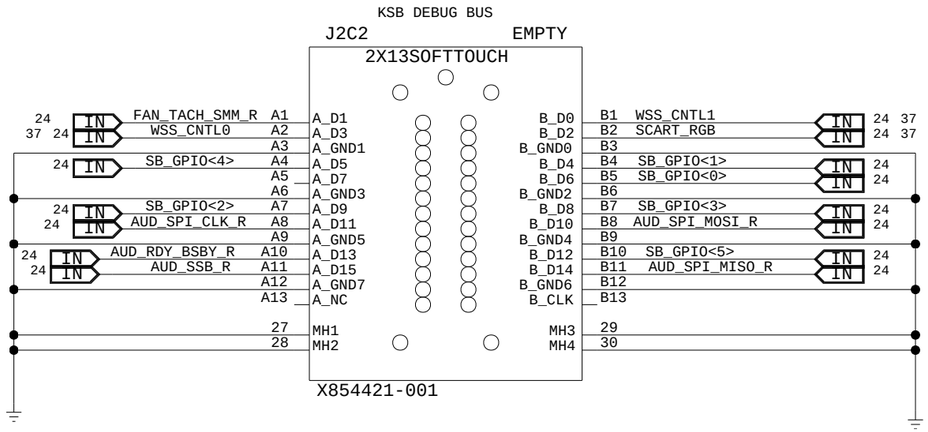
MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 61/74	FAB B	REV 1.0

XDK, DEBUG CONNECTORS

KSB DEBUG BUS

J2C2 EMPTY

2X13SOFTTOUCH

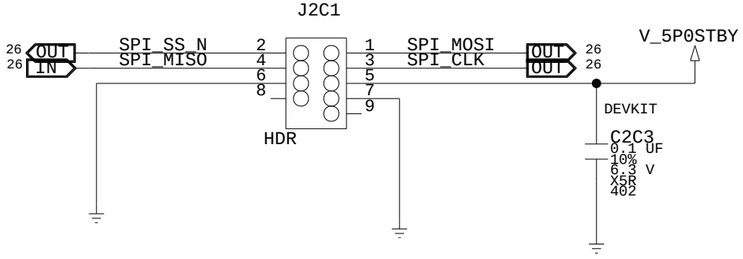


PHY MDIO INTERFACE

NET NAME	MDIO SIGNAL
SB_GPIO<1>	PCIE MDC
SB_GPIO<0>	PCIE MDIO
SB_GPIO<2>	FPHY MDIO
SB_GPIO<3>	FPHY MDC
SB_GPIO<5>	SATA0 MDC
SB_GPIO<4>	SATA0 MDIO
AUD_SPI_MOSI_R	SATA1 MDC
AUD_SPI_CLK_R	SATA1 MDIO
WSS_CNTL0	USGBRPA MDC
WSS_CNTL1	USGBRPA MDIO
AUD_RDY_BSBY_R	USGBRPB MDC
FAN_TACH	USGBRPB MDIO

DEVKIT

J2C1

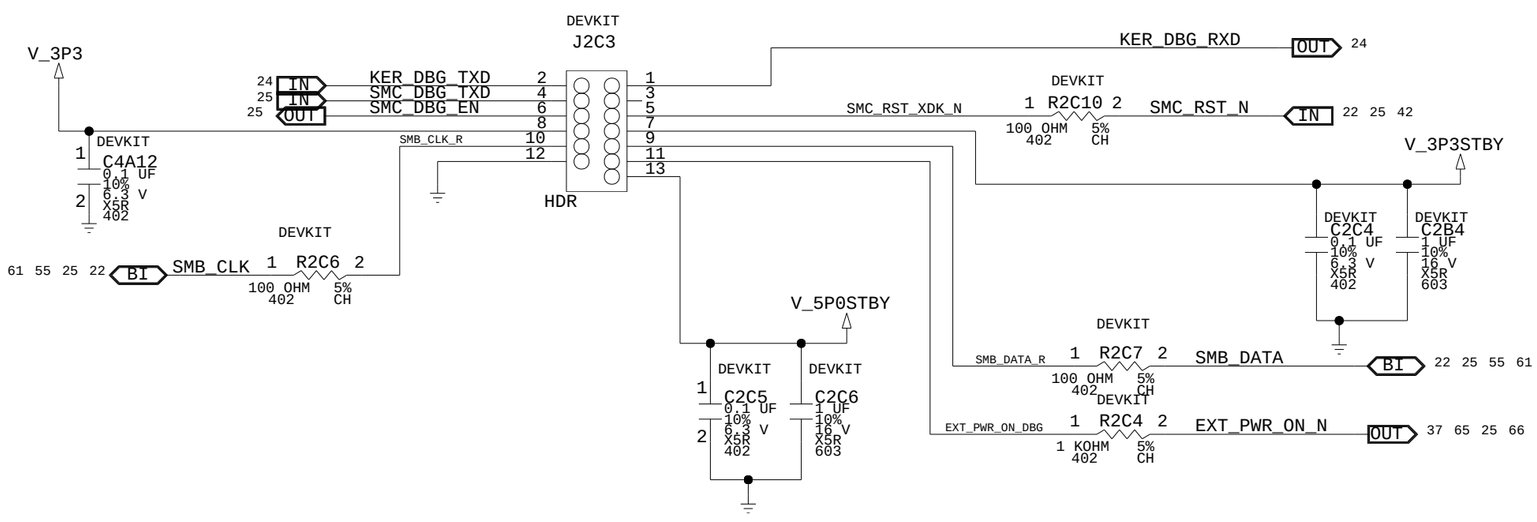


V_5P0STBY

V_3P3

DEVKIT

J2C3



[PAGE_TITLE=XDK. DEBUG CONN]

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Wed Mar 14 01:47:35 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 62/74	FAB B	REV 1.0

ALMOST BLANK

ALMOST BLANK

XDK DEBUG

GCPU JTAG HEADER
DEVKIT J4C1 2X4HDR
CPU_TDI, CPU_TDO, CPU_TCLK, CPU_TRST_N_R, CPU_TMS, GPU_TRST_N, GPU_TRST_ED_N
HDR

GCPU EEPROM HEADER
DEVKIT J4C3 2X3HDR
GPU_SROM_SCLK_R, GPU_SROM_SO_R, GPU_SROM_CS_N_R, GPU_SROM_SI, GPU_SROM_WP_N
HDR

SB JTAG HEADER
DEVKIT J3E2 2X3HDR
SB_TDI, SB_TDO, SB_TCLK, SB_TMS, SB_TRST
HDR

V_5P0DUAL
U2V1 DEVKIT IC SN74LVC1G14
DBG_LED0 → VCC/IN/GND, OUT/N/C
DBG_LED0_LED_R → DEVKIT R2V1 249 OHM 1% 402 CH → DBG_LED0_LED
DEVKIT D2G1 LED SM YELLOW
X801189-001

DEVKIT_RARE
U1D1 RCPT
FLSH_CE_N, FLSH_DATA<7>, FLSH_DATA<6>, FLSH_DATA<4>, FLSH_DATA<2>, FLSH_DATA<0>, MMC_RST_N, FLSH_WP_N, FLSH_DATA<5>, FLSH_DATA<3>, FLSH_DATA<1>

V_3P3STBY
DEVKIT C1R2 4.7 UF 10% 6.3 V X5R 603
DEVKIT C1R1 0.1 UF 10% 6.3 V X5R 402
DEVKIT C1R3 0.1 UF 10% 6.3 V X5R 402

V_3P3
DEVKIT C2F7 0.1 UF 10% 6.3 V EMPTY 402
DEVKIT C2F5 4.7 UF 10% 6.3 V X5R 805
USE VERSION 7-8
DEVKIT J2F1 1X3HDR
DEVKIT R2F6 CPU_PWRGD 5% 1 KOHM CH 402 → CPU_PWRGD_R

V_MEM
DEVKIT C4C4 0.1 UF 10% 6.3 V X5R 402
DEVKIT R4P8 10 KOHM 5% EMPTY 402

V_5P0
DEVKIT D4P1 GREEN SM 2 LED
CPU_CHECKSTOP_N_LED → DEVKIT R4P1 825 OHM 1% 402 CH → CPU_CHECKSTOP_N_LED_C

DEVKIT R4P2 1 KOHM 5% 402 CH
CPU_CHECKSTOP_N_LED_B → DEVKIT Q4C2 XSTR

V_3P3STBY
DEVKIT R3P1 10 KOHM 5% CH 402
SMC_CPU_CHKSTOP_DETECT → BI 25
DEVKIT R4C4 1 KOHM 5% 402 CH
SMC_CPU_CHKSTOP_DETECT_B → DEVKIT Q4C1 XSTR

USE VERSION 4-6
DEVKIT R4P3 1 KOHM 5% 402 EMPTY
CPU_RST_N_2_R
DEVKIT J4C2 2X5HDR
CPU_TMS, CPU_TRST_N, CPU_TDO, CPU_TDI, CPU_RST_V1P1_N, CPU_CHECKSTOP_N_R, CPU_CHECKSTOP_N, CPU_TCLK, EXT_PWR_ON_N
HDR
DEVKIT C4C3 0.1 UF 10% 6.3 V X5R 402
DEVKIT R4C7 0 OHM 5% 402 CH

PWR LEDS

V_12P0, V_5P0, V_5P0STBY, V_3P3, V_3P3STBY
DEVKIT R7A3 3.32 KOHM 1% CH 402 → V_12P0_LED_R → LED SM GREEN D7A1 DEVKIT
DEVKIT R2G8 1 KOHM 1% CH 402 → V_5P0_LED_R → LED SM GREEN D2G2 DEVKIT
DEVKIT R6A7 1 KOHM 1% CH 402 → V_5P0STBY_LED_R → LED SM GREEN D6A1 DEVKIT
DEVKIT R4A8 330 OHM 1% CH 402 → V_3P3_LED_R → LED SM GREEN D5A1 DEVKIT
DEVKIT R4B6 330 OHM 1% CH 402 → V_3P3STBY_LED_R → LED SM GREEN D4B1 DEVKIT

[PAGE_TITLE=XDK, DEBUG TITAN]

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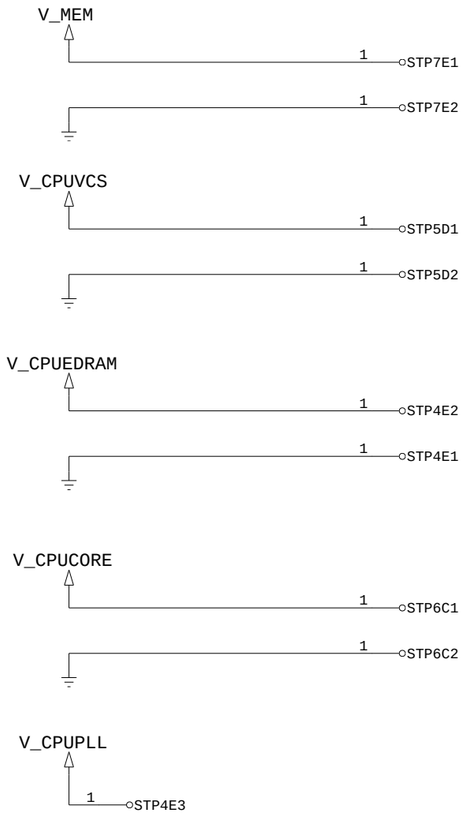
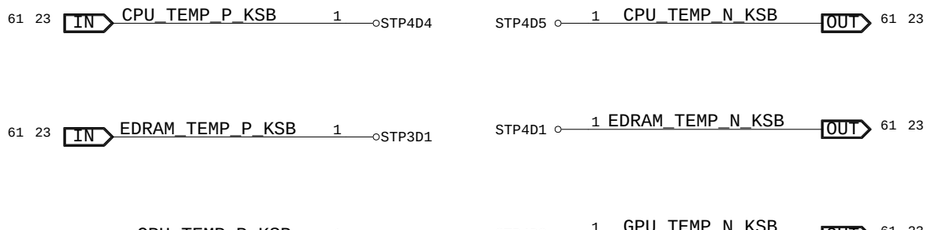
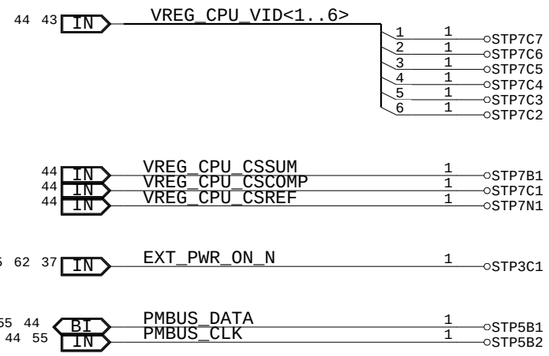
MICROSOFT CONFIDENTIAL	PROJECT NAME WAITSBURG	PAGE 65/74	FAB B	REV 1.0

DEBUG BOARD, SPYDER CONN

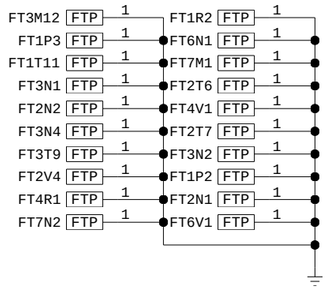
ALL STP POINTS SHALL BE ADDED TO TOP SIDE IN LAYOUT







GND FTS FOR TEST FIXTURES



[PAGE_TITLE=DEBUG BOARD, SPYDER CONN]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	66/74	B	1.0

LABELS AND MOUNTING

INTELLIGENT SERIAL NUMBER TARGET.

LB2B1
LABEL
1
EMPTY
X801181-001
BOM_IGNORE=TRUE

REF_DES	MS_PART#	MATERIAL	DESCRIPTION	BOM PROPERTY
LB2B1	X863442-001	1375X250_TARGET	LABEL,WAITSBURG	?

PACK_IGNORE=TRUE

WEST PCB MOUNTING HOLES

EDGE
MTG1B1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG1G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EDGE
MTG4G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

EAST PCB MOUNTING HOLES

EDGE
MTG7G1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

HEAT SINK MOUNTING HOLES

STD
MTG4F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG4D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6F1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

STD
MTG6D1
MTG_HOLE
NC9 9
EMPTY
GND=1,2,3,4,5,6,7,8

[PAGE_TITLE=LABELS AND MOUNTING]

DRAWING
Wed Mar 14 01:48:07 2012

POWER ARCHITECTURE

+12V
I=10.83A
P=130W

L1
0.4W
450nH/8A
Iin_max 5.8A
0.4W
2x470uF/
16V
Poly
10mOhm
4x4.7uF
1x1uF
MLCC

2.9A
1.62W
DPAK
1.38W
DPAK
1.15W
420nH/dual
Isat 40A
250KHz/ph
L2
1.38W
DPAK
0.12W
6x820uF/
2.5V
Poly
7mOhm

V_CPUCORE
0.9V-1.2V
43W TD/48A TD
51.6W Max/57A Max
54A TD
Min load 20%
η=82%

2.9A
1.62W
DPAK
1.15W
1.38W
DPAK
L2
1.38W
DPAK

+5POSTBY
I=1.0A
P=5W

0.09W
2.2uH
Iin_max 0.91A
3x10uF/
6.3V
MLCC
8mOhm
1x0.1uF/
16V
MLCC
xmOhm
V_5P0DUAL
1.5A TD
8.4W Max
DUALSO8
7W

0.06A
SOT23-5
0.24W
V_1P2STBY
0.20W TD/0.15A TD
0.24W Max/0.20mA Max
η=85%
0.1W
2.2uH/
1.7MHz
Isat 1.3A
1x10uF/
6.3V
MLCC
8mOhm

0.66A
SOT23-5
0.4W
V_3P3STBY
2.1W TD/0.64A TD
2.64W Max/0.80A Max
η=85%
0.08W
2.2uH/
1.7MHz
Isat 0.9A
1x10uF/
6.3V
MLCC
8mOhm

V_EFUSE
0.02A TD
0.03W TD
V_EFUSE(1.5V)
Linear SOT23
0.08W Max

Measured data shows
v_3p3 may be 330mA
less than budget

V_VCS
1.25-1.3V
12W TD/9.6A TD
13.2W Max/10.6A Max
η=82%

1.0 Ohm/
0.0625W
each, 0402

V_1P2
Linear DPAK
1.08W MAX
V_1P2
0.76A TD
0.9W TD

FB

L1
0.12W
450nH/8A
Iin_max 3.4A
3x4.7uF/
6.3V
MLCC
11mOhm
2x1uF/
6.3V
MLCC

0.5W
DPAK
1.21W*
(0.81W)
DPAK
L3
1.4W
1.7uH/
400KHz
Ipk 12.4A
820uF/
2.5V
Poly
7mOhm

V_5P0
5.09V,
43.3W TD/ 8.1A TD
47.6W Max/ 8.9 A
Max
Min load 50%
η=93%

0.91A
DUALSO8
1W
0.13W
2.3uH/600KHz
Isat 5.6A
L4
4x4.7uF/
6.5V
MLCC
8mohm

V_3P3
3.3V
2.88A TD
9.5W TD
10.56W Max
Min load 50%
η=88%

V_CPUPLL
0.45A TD
0.83W TD
V_1P83PLL
Linear DPAK
1.01W Max(loss)
V_1P83 Main
0.031A TD
0.057W TD
V_GPUPCIE
0.11A TD
0.165W TD
V_GPUPCIE(VTT)
(1.5V)
Linear SOT223
0.22W Max(loss)

L1
0.26W
450nH/8A
Iin_max 5.51A
0.18W
1x470uF/
16V
Poly
10mohm
4.6A
1x4.7uF
1x0.1uF
MLCC
1.4W
DPAK
1.4W
1.6uH 600KHz
Ipk 13A
L3
1.3W*
(1.05W)
DPAK
0.25W
820uF/
6.3V
E-Al
11mOhm

MICROSOFT CONFIDENTIAL
CORONA XDK MB POWER
ARCHITECTURE
MAX PWR4 DISSIPATION(+10%
LOAD)
JAN 12, 2010

Legend
Power rail from Switching Regulator
Power rail from External PSU
Power rail from Linear Regulator

0.91W*
*=using
same
FET like
HS

Expected
Airflow=0.3m/s

0.16W
450nH/8A
Iin_max 3.1A
L1
0.19W
1x470uF/
16V
Poly
10mohm
1x330uF/
16V
Poly
10mohm
4x4.7uF
1x1uF
MLCC

1.25A
0.98W
DPAK
1.5W*
(1W)
DPAK
1.2W
1.7uH/600KHz
Isat 11A
L3
2x820uF/
2.5V
Poly
7mohm
Option
1x820uF/
2.5V
Poly
7mohm

V_EDRAM
1.075V
9.7W TD/9A TD
10.6W Max/9.9A Max
Min load 50%
η=88%

1.9A
1W
DPAK
1.4W*
(1W)
DPAK
1.2W
1.7uH/600KHz
Isat 11.5A
L3
1x820uF/
2.5V
Poly
7mohm
Option
2x330uF
OsCon
7mOhm
Option
8x10uF
MLCC
11mOhm

V_MEM
1.8V
16W TD/9A
17.8W Max/10A max
Min load 50%
η=84%

<PAGE_TITLE=POWER ARCHITECTURE>

DRAWING
TRINITY_FAB_A
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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	68/74	B	1.0

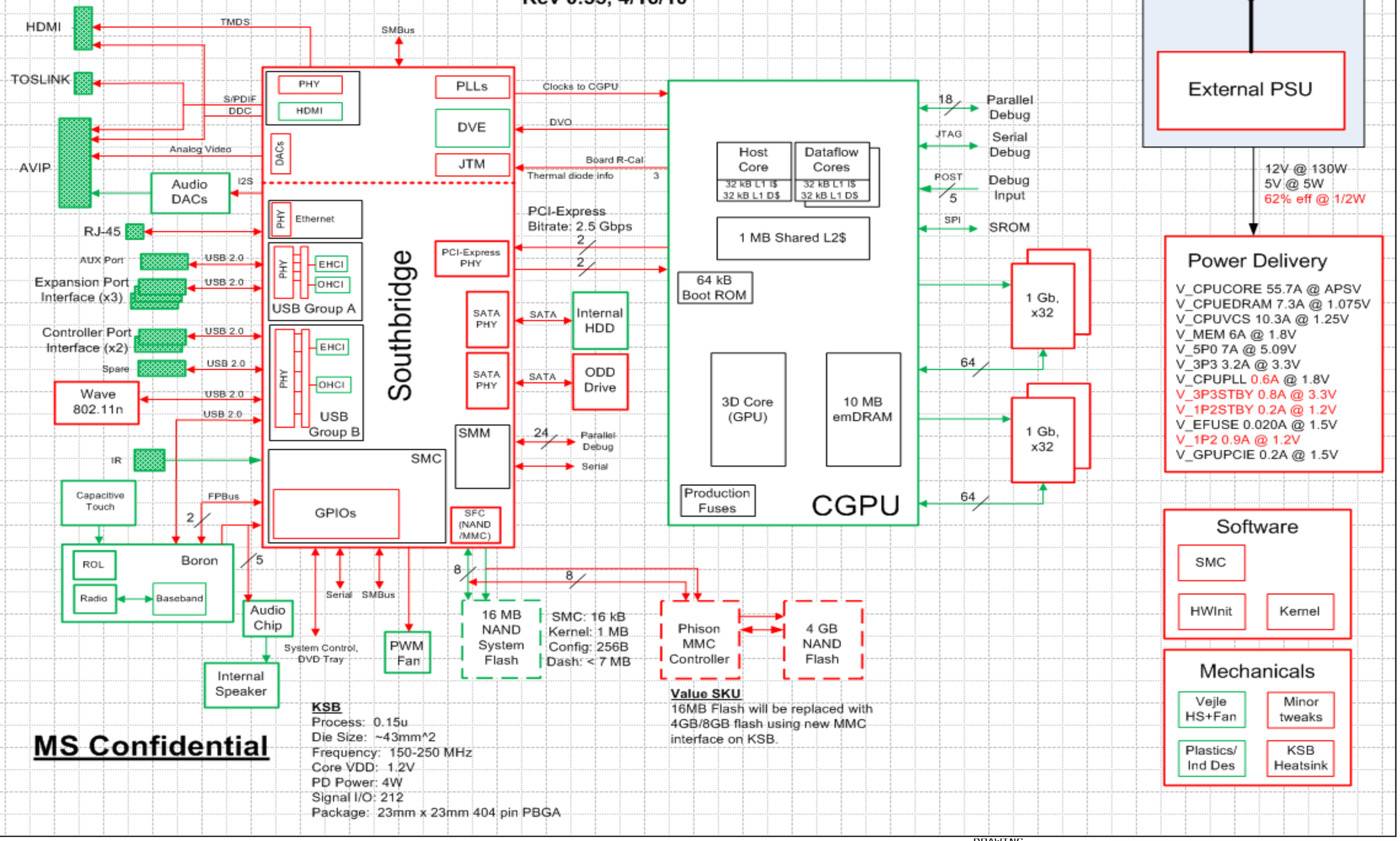
= No Change from Trinity, Regression Testing Only

= Change/New, Needs Special Attention on Corona

= Alternate Part Stuffing

Corona System

Rev 0.55, 4/16/10



KSB
Process: 0.15u
Die Size: ~43mm^2
Frequency: 150-250 MHz
Core VDD: 1.2V
PD Power: 4W
Signal I/O: 212
Package: 23mm x 23mm 404 pin PBGA

Value SKU
16MB Flash will be replaced with 4GB/8GB flash using new MMC interface on KSB.

MS Confidential

<PAGE_TITLE=SYSTEM BLOCK DIAGRAM>

DRAWING
TRINITY_FAB_A
Wed Mar 14 01:45:33 2012

MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	69/74	B	1.0

RESET/ENABLE DIAGRAM

WAVE CONN
USB TRIPPLE CONN
RJ45 AUX CONN
HDMI CONN
AVIP CONN
TOSLINK CONN
POWER CONN
AUDIO DAC
FAN CONN
HDD SATA CONN
ODD SATA CONN
ODD PWR CONN
HDD PWR CONN
STANDBY SWITCHERS VR
CPU VR
VCS VR
DEBUG CONN
V5P0 DUAL VR
V1P2 VR
GCPU
MEM A & B CLAM
KSB
FLASH
V5P0 V3P3 VR
VEFUSE VR
VGPUPCIE VR
V1P8 VR
VEDRAM VMEM VR
MEM C & D CLAM
TILT
PWR BUTTON
EJECT BUTTON
BORON FPM
IR
2 X GAME CONN

EXT_PWR_ON_N
AUD_RST_N
PSU_V12P0_EN
VREG_V1P2_EN
EXT_PWR_ON_N
SMC_DBG_EN
SMC_RST_N
VREG_CPU_EN
VREG_CPUCORE_PWRGD
CPU_RST_N
CPU_PWRGD
GPU_RST_N
GPU_RST_DONE
VREG_V5P0_EN
VREG_V3P3_EN
VREG_EFUSE_EN
VREG_VEDRAM_EN
VREG_VMEM_EN
MEM_RST
MEM_SCAN_EN
MEM_SCAN_TOP_EN
MEM_SCAN_BOT_EN
MEM_RST
MEM_SCAN_EN
MEM_SCAN_TOP_EN
MEM_SCAN_BOT_EN

COMPONENT STUFFING TABLES

MARGIN REF DES TO STUFF

REFDES	DBG/XDK	RETAIL
C1F2	STUFF	NO-STUFF
C1F10	STUFF	NO-STUFF
C1F11	STUFF	NO-STUFF
C1G7	STUFF	NO-STUFF
C1G8	STUFF	NO-STUFF
C1G9	STUFF	NO-STUFF
C1G10	STUFF	NO-STUFF
C1G11	STUFF	NO-STUFF
C1G12	STUFF	NO-STUFF
C1G13	STUFF	NO-STUFF
C1U2	STUFF	NO-STUFF
C2F2	STUFF	NO-STUFF
C2F4	STUFF	NO-STUFF
C2F6	STUFF	NO-STUFF
C2E4	STUFF	NO-STUFF
C2E5	STUFF	NO-STUFF
C2F6	STUFF	NO-STUFF
C3G11	STUFF	NO-STUFF
C3G2	STUFF	NO-STUFF
C3G4	STUFF	NO-STUFF
C3U2	STUFF	NO-STUFF
C3U3	STUFF	NO-STUFF
C3V2	STUFF	NO-STUFF
C4B1	STUFF	NO-STUFF
C4N1	STUFF	NO-STUFF
C4N4	STUFF	NO-STUFF
C5B15	STUFF	NO-STUFF
C5B5	STUFF	NO-STUFF
C5B8	STUFF	NO-STUFF
C5N7	STUFF	NO-STUFF
C5N8	STUFF	NO-STUFF
C6A6	STUFF	NO-STUFF
C6M5	STUFF	NO-STUFF
J1G3	STUFF	NO-STUFF
Q1F1	STUFF	NO-STUFF
Q2F3	STUFF	NO-STUFF
Q4B1	STUFF	NO-STUFF
R1F4	STUFF	NO-STUFF
R1F5	STUFF	NO-STUFF
R1F6	STUFF	NO-STUFF
R1G1	STUFF	NO-STUFF
R1T19	STUFF	NO-STUFF
R1U3	STUFF	NO-STUFF
R1U4	STUFF	NO-STUFF

MARGIN CONTINUED...

REFDES	DBG/XDK	RETAIL
R1U5	STUFF	NO-STUFF
R2B1	STUFF	NO-STUFF
R2B3	STUFF	NO-STUFF
R2F2	STUFF	NO-STUFF
R2F3	STUFF	NO-STUFF
R2F4	STUFF	NO-STUFF
R2F5	STUFF	NO-STUFF
R2F8	STUFF	NO-STUFF
R2T5	STUFF	NO-STUFF
R2U1	STUFF	NO-STUFF
R3E1	STUFF	NO-STUFF
R3E2	STUFF	NO-STUFF
R3E3	STUFF	NO-STUFF
R3E4	STUFF	NO-STUFF
R3F16	STUFF	NO-STUFF
R3F2	STUFF	NO-STUFF
R3F3	STUFF	NO-STUFF
R3F5	STUFF	NO-STUFF
R3G1	STUFF	NO-STUFF
R3G6	STUFF	NO-STUFF
R3G7	STUFF	NO-STUFF
R3G8	STUFF	NO-STUFF
R3G9	STUFF	NO-STUFF
R3N6	STUFF	NO-STUFF
R3U1	STUFF	NO-STUFF
R3U2	STUFF	NO-STUFF
R3U3	STUFF	NO-STUFF
R4B1	STUFF	NO-STUFF
R4B18	STUFF	NO-STUFF
R4B2	STUFF	NO-STUFF
R4B3	STUFF	NO-STUFF
R4N1	STUFF	NO-STUFF
R4N10	STUFF	NO-STUFF
R4N13	STUFF	NO-STUFF
R4N14	STUFF	NO-STUFF
R4N2	STUFF	NO-STUFF
R4N3	STUFF	NO-STUFF
R4N4	STUFF	NO-STUFF
R4N5	STUFF	NO-STUFF
R4N7	STUFF	NO-STUFF
R4N8	STUFF	NO-STUFF
R5B6	STUFF	NO-STUFF
R5N2	STUFF	NO-STUFF
R6A10	STUFF	NO-STUFF

MARGIN CONTINUED...

REFDES	DBG/XDK	RETAIL
R6A11	STUFF	NO-STUFF
R6M3	STUFF	NO-STUFF
R6M4	STUFF	NO-STUFF
U1F2	STUFF	NO-STUFF
U1F3	STUFF	NO-STUFF
U1G2	STUFF	NO-STUFF
U1U1	STUFF	NO-STUFF
U2U1	STUFF	NO-STUFF
U3E1	STUFF	NO-STUFF
U3E2	STUFF	NO-STUFF
U3G2	STUFF	NO-STUFF
U3G3	STUFF	NO-STUFF
U3T1	STUFF	NO-STUFF
U3V1	STUFF	NO-STUFF
U4B1	STUFF	NO-STUFF
U4B2	STUFF	NO-STUFF
U5B2	STUFF	NO-STUFF
U5B6	STUFF	NO-STUFF
U5N1	STUFF	NO-STUFF
U6A1	STUFF	NO-STUFF

PLEASE SEE BOM VARIANTS FOR STUFFING INSTUCTIONS
ON V1P2 AND STBY MARGINING

GDDR MEM. REFDES TO STUFF

REFDES	TOP ONLY (4GB)	TOP & BOT (8GB)
C5F1	STUFF	STUFF
C5U9	STUFF	STUFF
C6F3	STUFF	STUFF
C6U7	STUFF	STUFF
C7D12	STUFF	STUFF
C7E9	STUFF	STUFF
C7R6	STUFF	STUFF
C7T7	STUFF	STUFF
R5F5	STUFF	STUFF
R5T6	STUFF	STUFF
R5T7	STUFF	STUFF
R5U1	NO-STUFF	STUFF
R5U6	STUFF	STUFF
R6F5	STUFF	STUFF
R6R1	STUFF	STUFF
R6R2	STUFF	STUFF
R6T7	STUFF	STUFF
R6T8	STUFF	STUFF
R6T9	STUFF	STUFF
R6U1	NO-STUFF	STUFF
R7E1	STUFF	STUFF
R7E8	STUFF	STUFF
R7T1	NO-STUFF	STUFF
R7T6	NO-STUFF	STUFF
U5F1	STUFF	STUFF
U5U1	NO-STUFF	STUFF
U5U2	NO-STUFF	STUFF
U6F1	STUFF	STUFF
U6U1	NO-STUFF	STUFF
U7D1	STUFF	STUFF
U7E1	STUFF	STUFF
U7T1	NO-STUFF	STUFF
U7T1	NO-STUFF	STUFF

SROM MEMORY REFDES TO STUFF

REFDES	DEBUG	CPU DBG	XDK	RETAIL
C4R4	STUFF	STUFF	STUFF	NO-STUFF
R4R7	STUFF	STUFF	STUFF	NO-STUFF
R4R9	STUFF	STUFF	STUFF	NO-STUFF
R4R10	NO-STUFF	NO-STUFF	NO-STUFF	NO-STUFF
R4R11	STUFF	STUFF	STUFF	NO-STUFF
R4R12	STUFF	STUFF	STUFF	NO-STUFF

[PAGE_TITLE=COMPONENT STUFFING TABLES]

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MICROSOFT CONFIDENTIAL	PROJECT NAME	PAGE	FAB	REV
	WAITSBURG	71/74	B	1.0

I2C REFERENCE TABLES

DIGITAL POTENTIOMETERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESS
VMEM	256	0.007031V	W: 01011000 0X58, R: 01011001 0X59
VEDRAM	256	0.004199V	W: 01011000 0X58, R: 01011001 0X59
V5P0	256	0.011719V	W: 01011010 0X5A, R: 01011011 0X5B
V3P3	256	0.008V	W: 01011010 0X5A, R: 01011011 0X5B
VREF	256	0.007031V	W: 01011110 0X5E, R: 01011111 0X5F
VCS	256	?V	W: 01011110 0X5E, R: 01011111 0X5F
GPUPCIE	256	0.005859V	W: 01011100 0X5C, R: 01011101 0X5D
CPUPLL_1P8	256	0.007148V	W: 01011100 0X5C, R: 01011101 0X5D
V1P2STBY	?	?V	W: 01010100 0X54, R: 01010101 0X55
V3P3STBY	?	?V	W: 01010100 0X54, R: 01010101 0X55
V1P2	?	?V	W: 01010110 0X56, R: 01010111 0X57

STEPS/STEPSIZE TB UPDATED

ANALOG TO DIGITAL CONVERTERS

VOLTAGE RAIL	STEPS	STEP SIZE	I2C R/W ADDRESS
VMEM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
VEDRAM	4096	0.001221V	W: 01010000 0X50, R: 01010001 0X51
V5P0	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
V3P3	4096	0.000806V	W: 01010010 0X52, R: 01010011 0X53
VCS	4096	0.000806V	W: 01001000 0X48, R: 01001001 0X49
MEM_VREF	4096	0.000806V	W: 01000110 0X46, R: 01000111 0X47
GPUPCIE	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
CPUPLL_1P8	4096	0.000806V	W: 01000010 0X42, R: 01000011 0X43
V12P0	?	?V	W: 10000000 0X80, R: 10000001 0X81
TEMP SENSOR	?	?V	W: 10011100 0X9C, R: 10011101 0X9D
V5P0STBY	?	?V	W: 10011000 0X98, R: 10011001 0X99
V1P2STBY	?	?V	W: 10000110 0X86, R: 10000111 0X87
V3P3STBY	?	?V	W: 10010010 0X92, R: 10010011 0X93
V1P2	?	?V	W: 10000010 0X82, R: 10000011 0X83

STEPS/STEPSIZE TB UPDATED

WAITSBURG DOC TRACKER

Document#	Document Title
H104359	Waitsburg Document Tree
H101502	Corona Game Console Product Specification
H08676	Console Usage Model And Reliability Budget
H101667	Corona Console Specifications Template
H101671	Corona System Block Diagram
H09424	Vjele Datasheet
H08769	Trinity Console PLL Specification
H101637	Southbridge Security Review
H101786	KSB Programmer's Model
H101787	KSB Register Specification
H101665	Corona Power On Reset Timing Diagram
H08754	Trinity Console Audio / Video Specification
H101664	Corona SMC Firmware Requirements
H102138	Winchester Console Flash Specification
H104793	DataIO Flash Programming Job Creation for Waitsburg eMMC
H104815	Waitsburg Console USB Specification
H08770	Trinity Console Tilt Switch Specification
H09297	Spec,System Fan,High Speed PWM
H09169	Specification,RJ45+Auxiliary Power Connector
H08776	Trinity Console FPM Requirements Document
H08775	Trinity Console FPM LED Display Spec
H09443	Boron Front Panel Module Product Specification
H100727	Trinity Front Panel Module SMC Serial Protocol Specification
H101005	Wave Module Specification
H09553	802.11n Wi-Fi Module Supplier Qualification Requirements
H08757	Trinity Console IR Specification
H02235	Spec,Xenon,Optical Disc Drive Anti Piracy Specification
H08938	Xbox360 Optical Disc Drive Component Specification,Mustang
H08939	Xbox360 Optical Disc Drive Interface Specification,Mustang
H08753	Hard Drive Component Specification
H101663	Corona System Power Budget
H101672	Corona 1/2w Standby Power Budget
H101662	Corona Console VR Architecture
H101572	Spec,ACPT,Sys PS,120w,Small Form Factor;2-Outp W/Fan,1/2w
H08945	Spec,DC Output Cord Assy Acceptance Specification,Dual Barrel
?H08758	Trinity Console V_CPUCORE Regulator Specification (Obsolete?)
H08762	Trinity Console V_5P0 Regulator Specification
H08763	Trinity Console V_3P3 Regulator Specification
H08765	Trinity Console V_EDRAM Regulator Specification
H08764	Trinity Console V_MEM Regulator Specification
H08759	Trinity Console V_CPUVCS Regulator Specification
H101661	Corona Console Linear Regulators Specification
H101659	Corona Console V_3P3STBY Regulator Specification
H101660	Corona Console V_1P2STBY Regulator Specification
H05204	Spec,Xenon PCB Specification,TG150
H07678	Specification Odin Mechanical Design

[PAGE_TITLE=DOC TRACKER]

Change list

- started from Corona Fab E

Sep 26, 2011
- retail:p3, removed CPU_DBGx_POSTx connections to FTPs
- all:p22, modified R3R5 because of updated .ptf entry (was X814857-001, is X814857-001) (was 84.52 KOHM, is 84.5 KOHM)
- all:p30, modified FB2R1 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)
- all:p31, modified FB3P2 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)
- all:p31, modified FB3P1 because of updated .ptf entry (was X857387-001, is X857387-001) (was 0.45 OHM, is 0.45DCR)
- all:p35, modified SW5G2 because of updated .ptf entry (was X800550-004, is X800550-004) (was SM, is TH)
- all:p35, modified SW3G1 because of updated .ptf entry (was X850477-001, is X850477-001) (was _, is SPST)
- all:p38, modified FB2M1 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)
- all:p39, modified FB1A1 because of updated .ptf entry (was X801122-001, is X801122-001) (was 0.5A, is 500)

Oct 11,2011
- all:p26, added series term to FLSH_DATA<0:7>,FLSH_WP_N,FLSH_CLE,FLSH_CE_N
- all:p26, replaced stitching caps to 25v
- all:p32, removed Phison,NAND, added eMMC
- all:p34, connected NAND after the series term
- all:p33, replaced WM1824 with WM1824B
- all:p44, replaced NCP4201 with NCP4202
- all:p39, combined V_GAMEPORT2 with V_GAMEPORT1,replaced thermistor with X800753-001,removed V_GAMEPORT2 thermistor
- all:p39, combined V_EXPPORT2 with V_EXPPORT1, replaced thermistor with X800753-001, removed V_EXPPORT2 thermistor
- all:p39, updated usbtriple connector symbol

Oct 21, 2011
- xdk:p1, title page
- retail:p1, title page
- xdk:p2, MATERIAL=EMPTY:R4P5,R4P4, BOM=DEVKIT:R4R20, BOM=GCPU_VEJLE_BASE:U5E1
- all:p4, BOM=GDDR_BOTTOM:U5U2,R6U6
- all:p5, BOM=DEVKIT: all parts this page
- all:p9: removed BOM=CORE: all parts this page
- all:p10: removed BOM=CORE: all parts this page
- all:p11: removed BOM=CORE: all parts this page
- all:p14: MATERIAL=EMPTY: U7E1, added PART_LINE_ITEMs for U7E1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7T4, added PART_LINE_ITEM for R7T4
- all:p15: MATERIAL=EMPTY: U7T1, added PART_LINE_ITEMs for U7T1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7E7, added PART_LINE_ITEM for R7E7, BOM=GDDR_BOTTOM:R7T6
- all:p16: MATERIAL=EMPTY: U7D1, added PART_LINE_ITEMs for U7D1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7R4, added PART_LINE_ITEM for R7R4
- all:p17: MATERIAL=EMPTY: U7R1, added PART_LINE_ITEMs for U7R1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R7D5, added PART_LINE_ITEM for R7D5, BOM=GDDR_BOTTOM:R7T1
- all:p18: MATERIAL=EMPTY: U5F1, added PART_LINE_ITEMs for U5F1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R5U4, added PART_LINE_ITEM for R5U4
- all:p19: MATERIAL=EMPTY: U5U1, added PART_LINE_ITEMs for U5U1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R5F2, added PART_LINE_ITEM for R5F2, BOM=GDDR_BOTTOM:R5U1
- all:p20: MATERIAL=EMPTY: U6F1, added PART_LINE_ITEMs for U6F1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R6U4, added PART_LINE_ITEM for R6U4
- all:p21: MATERIAL=EMPTY: U6U1, added PART_LINE_ITEMs for U6U1, BOM=GDDR_TOP_SAMSUNG&GDDR_TOP_WINBOND:R6F2, added PART_LINE_ITEM for R6F2, BOM=GDDR_BOTTOM:R6U1
- all:p24: BOM=RETAIL:R2C12, BOM=DEVKIT:R2C11
- all:p25: BOM=RETAIL:R2G4, BOM=DEVKIT:R2G3, BOM=JTM_INT:R3R12, BOM=JTM_EXT:R3R10
- all:p35: BOM=DEVKIT:SW3G1
- xdk:p38: BOM=DEVKIT:R7A1,R7A2,R6B1
- all:p45: X857866-001:Q6B2,Q6B1, X857867-001:Q6C2,Q6C1,Q5C3,Q5C1
- all:p47: X857866-001:Q2F1, X857867-001:Q2F2, BOM=DEVKIT:R2G1, BOM=VREG_FIXED:R2E4,R2T4, X821117-001:R2E5, X801000-001:R2F1
- all:p48: BOM=DEVKIT:R1F19, BOM=VREG_FIXED:R1E20, BOM=VREG_FIXED:R1E19
- all:p49: X857866-001:Q3F1, X857867-001:Q4F1, BOM=DEVKIT:R4F1, BOM=VREG_FIXED:R3F8,R3F9, Part# change:C3F3,C3F2,R3F6,R3F10,R3F7,R3V1
- all:p50: X857866-001:Q7G1, X857867-001:Q7G2, BOM=DEVKIT:R7F1, BOM=VREG_FIXED:R3G11,R3G12, Part# change:C3G7,C3G6,R3V4,R3G13,R3G10,R4G3
- all:p51: X857866-001:Q5B1, X857867-001:Q5C2, BOM=DEVKIT:R5C2, BOM=VREG_FIXED:R4B17,R4B19
- all:p52: BOM=RETAIL:R4B14, added PART_LINE_ITEM for R4B14, BOM=VREG_FIXED:R4B9,R4B7,R4E8,R4E6
- all:p53: BOM=DEVKIT:R4B7,R5A11, BOM=VREG_FIXED:R5B5,C5B1,R5A15,R5A6,C5A1,R5A5, added PART_LINE_ITEMs, BOM=VREG_MM:R5B2,R5A13,R5A8,R5A12
- all:p54: MATERIAL=EMPTY:C7M1,C4N8,C2V2,C3E2,C3C7,C1U3,C4N2
- all:p55: BOM=DEVKIT:R3B1,R3B2,J5B1, BOM=RETAIL:R3C2,R3C1, BOM=VREG_MM: various parts
- all:p56: BOM=VREG_MM: various parts
- all:p57: BOM=VREG_MM: various parts
- all:p58: BOM=VREG_MM: various parts
- all:p59: BOM=VREG_MM: various parts
- all:p60: BOM=VREG_MM: various parts
- all:p61: BOM=JTM_INT: various parts, BOM=JTM_EXT: various parts
- all:p62: BOM=DEVKIT: all parts this page
- all:p65: BOM=DEVKIT: various parts
- all:p67: MATERIAL=EMPTY:LB2B1, added PART_LINE_ITEM for LB2B1
- all:p73: updated to Waitsburg Document tree
- all:p74: this page

Dec 26, 2011
- all:p32: changed R1D4 from X801814-001 to X806693-001
- all:p53: changed R5A4 from NO-STUFF to STUFF, changed R5A7,C5M8,C5M5 to NO-STUFF

Schematic Transitions for Waitsburg

This document lists the schematic changes needed to transform Waitsburg Fab A from Debug to XDK to Retail.
The base schematic is Waitsburg Fab A Debug

Waitsburg Debug to XDK changes
Start from Waitsburg Fab A Debug and replace the following files/pages:
page1.csa: Rename title page to XDK
page12.csa: Delete nets MA_A<12>, MB_A<12>
page13.csa: Delete nets MC_A<12>, MD_A<12>
page14.csa: Delete nets MA_A<12>, stuff R7T5,R7T4 (MEM_A_VREF1 resistor divider)
page15.csa: Delete nets MA_A<12>, stuff R7E6,R7E7 (MEM_A_VREF0 resistor divider)
page16.csa: Delete nets MB_A<12>, stuff R7R2,R7R4 (MEM_B_VREF1 resistor divider)
page17.csa: Delete nets MB_A<12>, stuff R7D4,R7D5 (MEM_B_VREF0 resistor divider)
page18.csa: Delete nets MC_A<12>, stuff R5U5,R5U4 (MEM_C_VREF1 resistor divider)
page19.csa: Delete nets MC_A<12>, stuff R5F1,R5F2 (MEM_C_VREF0 resistor divider)
page20.csa: Delete nets MD_A<12>, stuff R6U5,R6U4 (MEM_D_VREF1 resistor divider)
page21.csa: Delete nets MD_A<12>, stuff R6F1,R6F2 (MEM_D_VREF0 resistor divider)
page62.csa: Delete MEM_VREFS shunt circuitry
page63.csa: blank, deleted entire page
page64.csa: blank, deleted entire page

Waitsburg XDK to Retail changes
Start from Waitsburg Fab A XDK and replace the following files/pages:
page1.csa: Rename title page to RETAIL
page2.csa: Delete CPU_TE pulldown resistor (R4R20) and tie U5E1.E7 to ground
page3.csa: Disconnect U5E1 TB[0:7],TB[11:15] from CPU_DBG<0..15> bus, ground FTPs for TB[0:7], float FTPs for TB[11:15]
page5.csa: Diconnect U5E1.E3 (SROM_EN) from pullup resistor (R4R2)
page25.csa: Short U3D1.A6 (SMC_UART1_RXD) to V_3P3STBY
page38.csa: Delete V_12P0 shunt resistors (R7A1,R7A2), short V_12P0 to J7A1 pins 5-8. Remove short_parts (ST7A1,ST7A2).
page38.csa: Delete V_5P0STBY shunt resistor (R6B1), short V_5P0STBY to J7A1.10. Remove short_parts (ST6B1,ST6B2)
page47.csa: Delete V_5P0 shunt resistor (R2G1), short V_5P0 to L2F1.2. Remove short_parts (ST2G2,ST2G3)
page48.csa: Delete V_3P3 shunt resistor (R1F9), short V_3P3 to L1F1.2. Remove short_parts (ST1F1,ST1F3)
page49.csa: Delete V_CPUEDRAM shunt resistor (R4F1), short V_CPUEDRAM to L4F1.2. Remove short_parts (ST4F2,ST4F4)
page50.csa: Delete V_MEM shunt resistor (R7F1), short V_MEM to L7F1.1. Remove short_parts (ST7F2,ST7F3)
page51.csa: Delete V_CPUVCS shunt resistor (R5C2), short V_CPUVCS to L5C1.2. Remove short_parts (ST5C1,ST5C3)
page52.csa: Delete V_5P0 shunt resistor (R2G1), short V_5P0 to L2F1.2. Remove short_parts (ST2G2,ST2G3)
page53.csa: Delete V_1P2 shunt resistor (R4B14), short V_1P2 to U3B1.4. Remove short_parts (ST4B1,ST4B2). Remove PART_LINE_ITEM FOR R4B14
page53.csa: Delete V_GPUPCIE shunt resistor (R4E11), short V_GPUPCIE to U4E2 pin 2 and 4.
page53.csa: Delete V_1P8 shunt resistor (R4E12), short V_1P8 to U4E1.2. Delete V_CPUPLL shunt resistor (R4E4) replace with short_part
page53.csa: Delete V_EFUSE shunt resistor (R4P10), short V_EFUSE to U4P2.5.
page62.csa: Delete PCIe mid-bus probe (J3E1). Delete GPU_CLK probe (J4D2). Delete SMC_DBG_RXD filter (R2C2,C2C1). Float J2C3.3
page65.csa: Delete DBPADs to V_5P0, V_3P3, GND

Caveat:
On the Waitsburg Debug, page 38, there is a thermistor, RT3B1. This thermistor is the same thermistor on Waitsburg Retail, page 38, RT3A2.
During layout, ref des were renumbered on the Waitsburg Retail schematic page.
TO DO: Respin Waitsburg Retail schematic and fab and change RT3A2 to RT3B1
TO DO: Respin Waitsburg Retail schematic and fab and change RT3A2 to RT3B1
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TO DO: Respin Waitsburg Retail schematic and fab and change RT3A2 to RT3B1

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